PYNQ-ZU

Reference Manual v1.2

Revision HistoryV1.2

07/09/2021

Data	Version	Revision
07/31/2020	V1.0	• Updated Logo • Updated Contents, Added Hierachy • Put credits and reference for pictures used • Add intended audience, • Add intended applications, • Add tool support – PYNQ, Vitis, Vitis AI and Vivado • Replace with Board requirements document diagram • Update the board picture
06/17/2021	V1.1	• Updated Contents • Update final image • Add labels for main components • Add Board Component Description • Updated Block Diagram of Board • Add image/diagram of HDMI ports • Add diagram of WIFI-BT • Add image of USB3.0 ports • Add image/diagram of AUDIO ports • Add Standard Peripheral of SYZYGY ports • Add image/diagram of XADC ports • Delete all schematics
07/09/2021	V1.2	• Updated Figure 3-3 • Add form of Raspberry Pi GPIOs

Table of Contents

Introduction

Overview

The PYNQ-ZU is a Zynq® UltraScale+™ XCZU5EG-1SFVC784 MPSoC development board designed to be used with the PYNQ™open-source framework.

To find out more about PYNQ, please see the project webpage at www.pynq.io. Here you will find materials to help you get started with PYNQ and a forum for contacting the supporting community.

The photo of the platform is shown below Figure 1-1

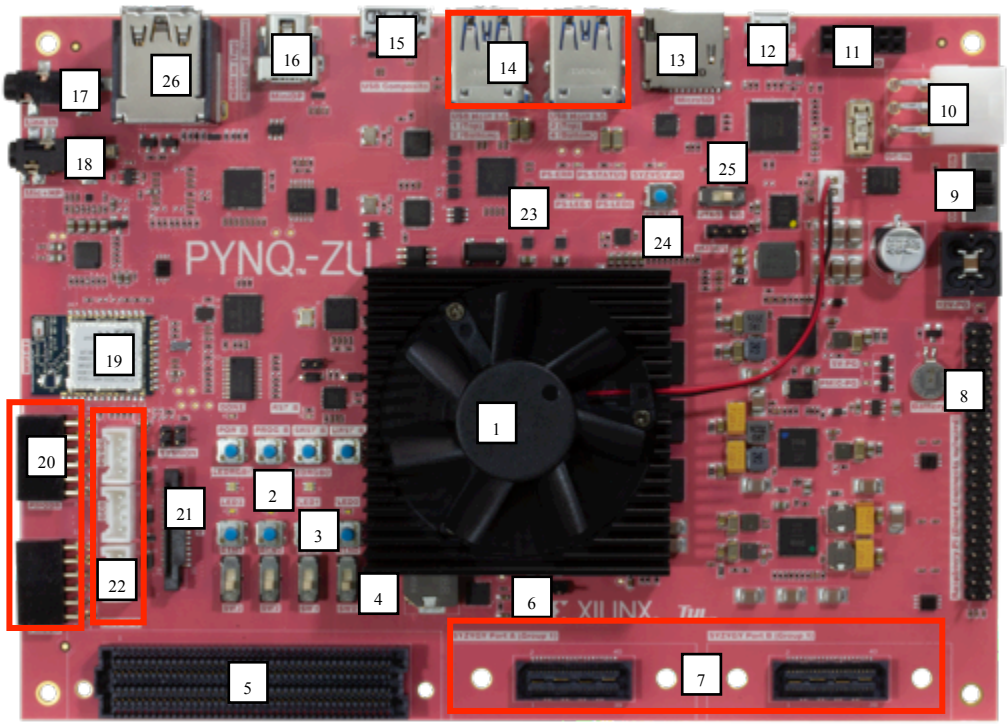


Figure 1-1

Table : PYNQ-ZU Board Component Description

Callout	Component Description
1	XCZU5EG-1SFVC784
2	LEDs(x4,PL),LED RGB(x2,PL)
3	Button(x4,PL)
4	Switch(x4,PL)
5	FMC-LPC
6	ADC
7	SYZYGY Standard connector (x2)
8	40-Pin Raspberry PI connector
9	Power switch
10	Power-IN
11	Pmod (x1 PS Pmod-TPM)
12	Micro USB UART
13	MicroSD
14	USB 3.0 Hub
15	Composite USB 3.0
16	Mini Display Port
17	Audio (MIC+HP)
18	Audio (LINE-IN)
19	Wifi + BT
20	Pmod (x2)
21	MIPI CSI
22	Grove connectors (x3)
23	LEDs (x2,PS)
24	Button(x1,PS)
25	JTAG-SD boot mode switch
26	HDMI Video TX & RX (banked)

Target User

The board supports the following developer and user persona:

- Hardware designers who want to design a system, at an RTL or system level, using Vivado IPI tools, to use the interfaces available on the board
- Embedded software engineers who like to develop embedded systems using Vivado IPI, Vivado/Vitis HLS, and Vitis embedded development software
- Domain experts software engineers/developers who like to develop applications in Python using PYNQ framework or C/C++ language

Target Applications

- parallel hardware execution
- high frame-rate video processing
- hardware accelerated algorithms
- real-time signal processing
- high bandwidth IO
- low latency control

Tools Support

The PYNQ-ZU platform is supported by the PYNQ framework, and Vitis, Vitis AI, and Vivado tools.

Block Diagram

The PYNQ-ZU board block diagram is shown in Figure 1-2.

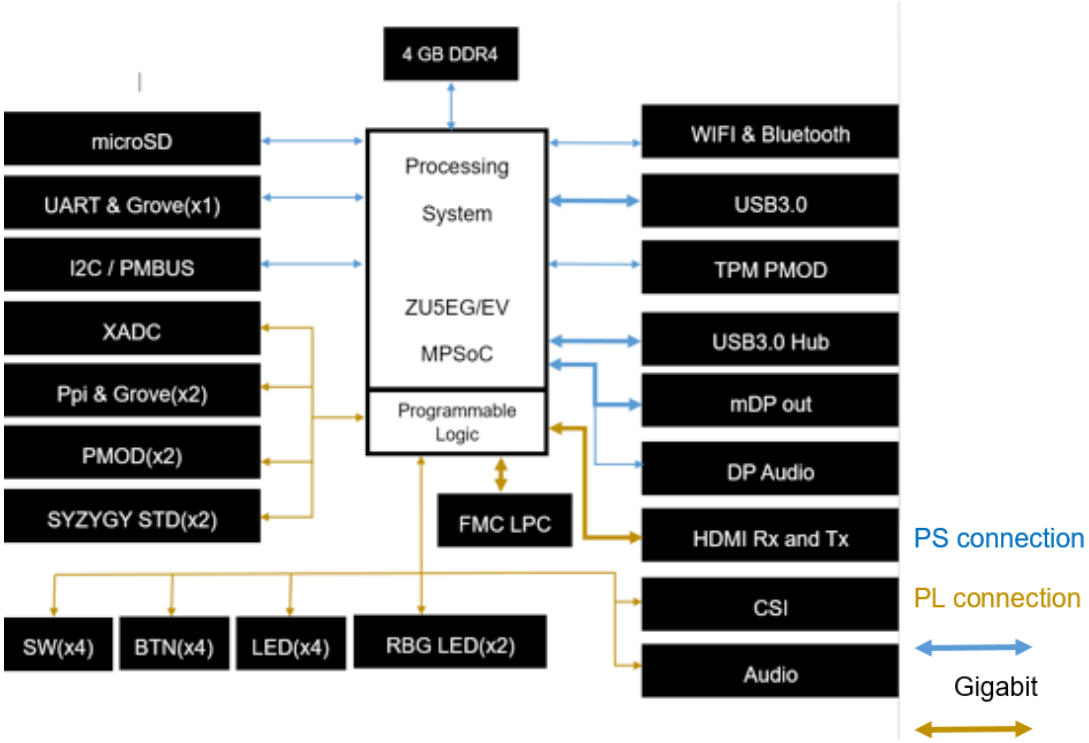


Figure 1-2

Board Features

The PYNQ-ZU board features are listed here. Detail information for each feature is provide in Board Component Descriptions.

Device: Zynq Ultrascale+™ MPSOC XCZU5EG-1SFVC784
FPGA Clocks

- PL-Clocks
- User-Clock
- GTR-USB3.0-Clock
- GTR-DP-Clock

PS Connected peripherals

- Micro USB UART
- MicroSD
- 4GB DDR4
- Composite USB 3.0
- USB 3.0 Hub
- Mini Display Port
- Wifi + BT
- User LEDs (x2)
- XADC pins (x2)
- Pmod (x1 PS Pmod-TPM)
- Grove connectors (x1)

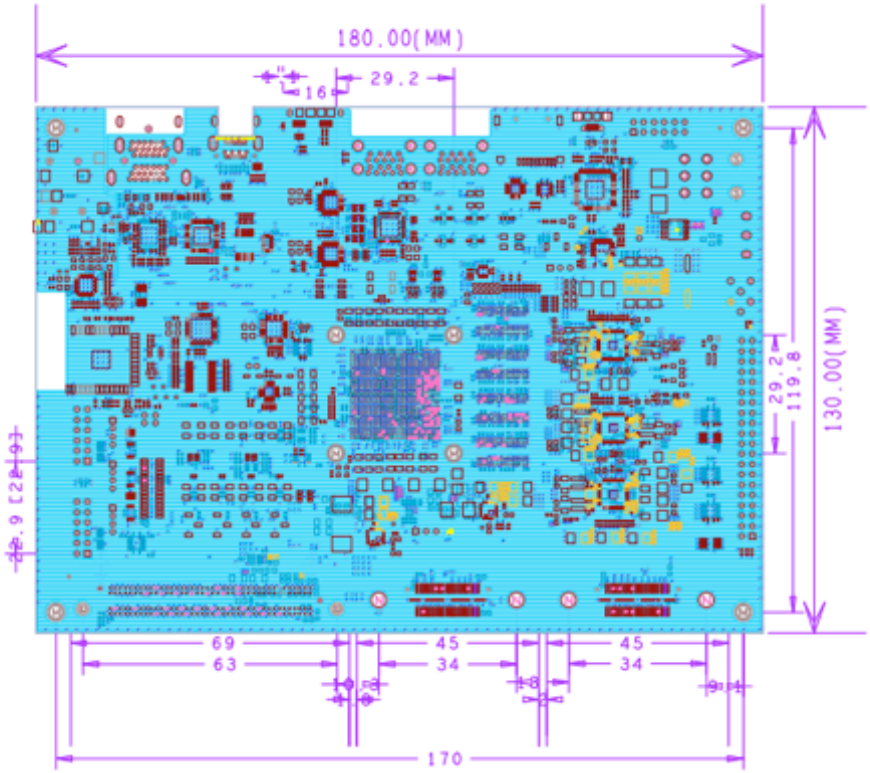
PL Connected peripherals

- Audio (MIC+HP, Line In)
- HDMI Video TX
- HDMI Video RX
- RGB LEDs (x2)
- User LEDs (x4)
- DIP switches (x4)
- Pushbuttons (x4)
- MIPI CSI
- Pmod (x2)
- FMC LPC
- SYZYGY Standard connector (x2)
- Grove connectors (x2)
- 40-Pin Raspberry PI connector

Board Specifications

Dimensions

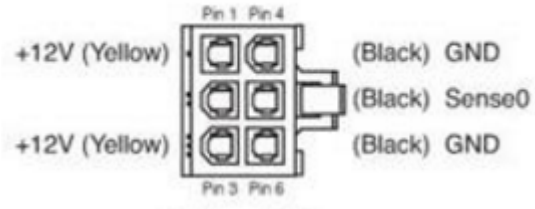
Width: 180mm
Length:130mm



Board Component Descriptions

Power

The PYNQ-ZU must be powered from an external 12V DC power supply. The Power Jack is DC-IN.



Power switch is shown in Figure 3-1.

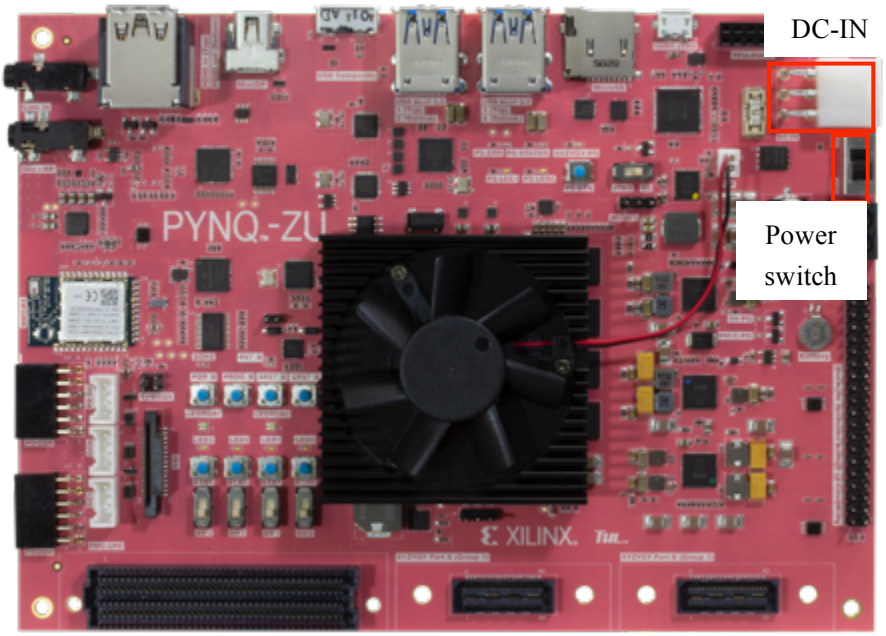


Figure 3-1

Boot mode selection

The PYNQ-ZU supports MicroSD and JTAG boot modes. The boot mode is selected using the JTAG SD DIP switch. To select the JTAG mode, slide the switch to the left. To select MicroSD mode, slide the switch to the right. The switch is shown in Figure 3-2.

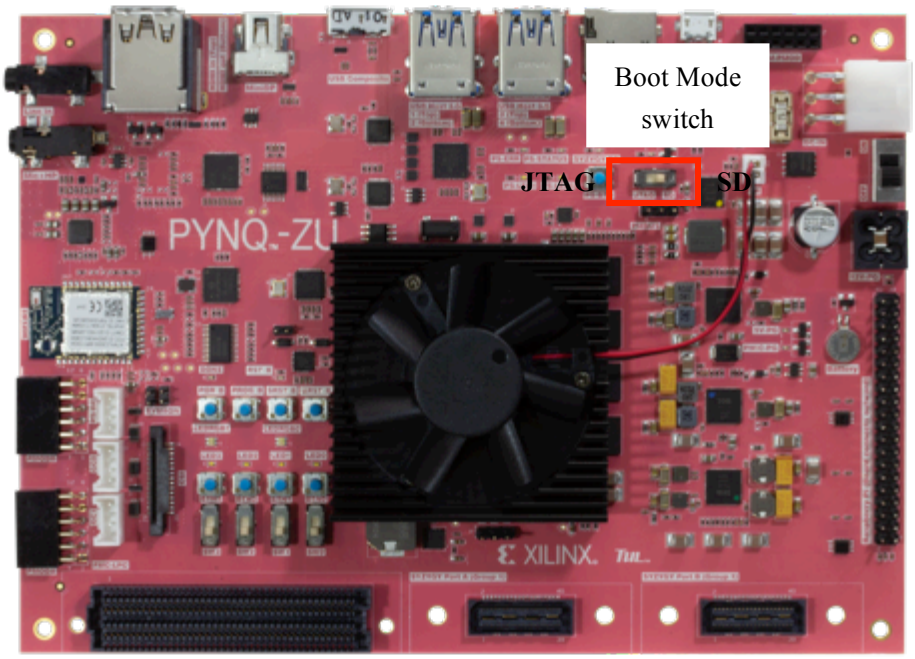


Figure 3-2 Boot Mode Switch

PS connected peripherals

Clock Sources

The PYNQ-ZU board provides fixed clock sources for XCZU5EG MPSOC. Table 3-1 lists various clock names, their frequencies, and the clock sources used to generate them. Table 3-2 lists FPGA pins to which the generated clocks are sourced.

Table 3-1

Clock Name	Frequency	Clock Source
Fixed Frequency Clock		
GTR_REF_DP_CLK	27MHz	Si5340A Clock Generator
GTR_REF_USB30_CLK	26MHz	
FPGA_CLK125	125MHz	
FPGA_USER_CLOCK	156.25MHz	
PS_REF_CLK	33.333MHz	OSC

Table 3-2 Clock Connections, Source to XCZU5EG MPSOC

Schematic Net Name	FPGA Pin
GTR_REF_DP_CLK_P	E21
GTR_REF_DP_CLK_N	E22
GTR_REF_USB30_CLK_P	F23
GTR_REF_USB30_CLK_N	F24
FPGA_CLK125_P	K4
FPGA_CLK125_N	K3
FPGA_USER_CLOCK_P	AD5
FPGA_USER_CLOCK_N	AD4

DRAM

The PYNQ-ZU includes four Micron 512Mx16 DDR4 memory.
Each MT40A512M16JY-083E has a 16-bit wide interface with a total capacity of 1GB. The four modules combine to provide a 64-bit data path. The DDR4 is connected to the hard memory controller in the Processor Subsystem (PS).

The PS DDR4 memory controller supports speeds of up to 2400MT/s on the PYNQ-ZU board.

The DDR4 configuration of the PYNQ-ZU board is shown in Figure 3-3.

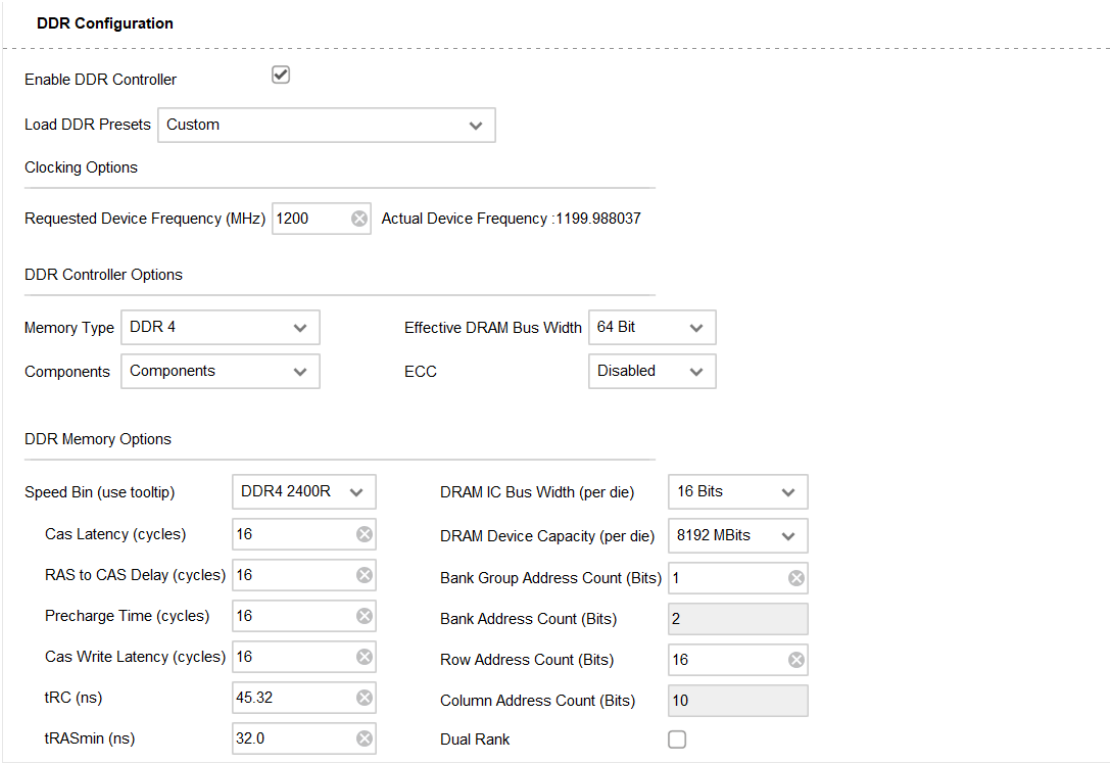


Figure 3-3 DDR4 Configuration in Vivado

Micro SD

The PYNQ-ZU has a MicroSD slot (SD0). An SD card can be used to boot the board, or for applications that require non-volatile external memory storage.

MIO	Name
13	MIO13_SDIO_D0
14	MIO14_SDIO_D1
15	MIO15_SDIO_D2
16	MIO16_SDIO_D3
21	MIO21_SDIO_CMD
22	MIO22_SDIO_CLK
24	MIO24_SDIO_CD

PS I2C MUX

The PS-side I2C0 interface provides access to I2C peripherals through a set of I2C . The system controller connected to the PL-side by the I2C0_SDA/SCL Bus. Figure 3-4 shows a high-level view of the I2C0 bus connectivity represented in below table. TCA9548A is set to 0x75.

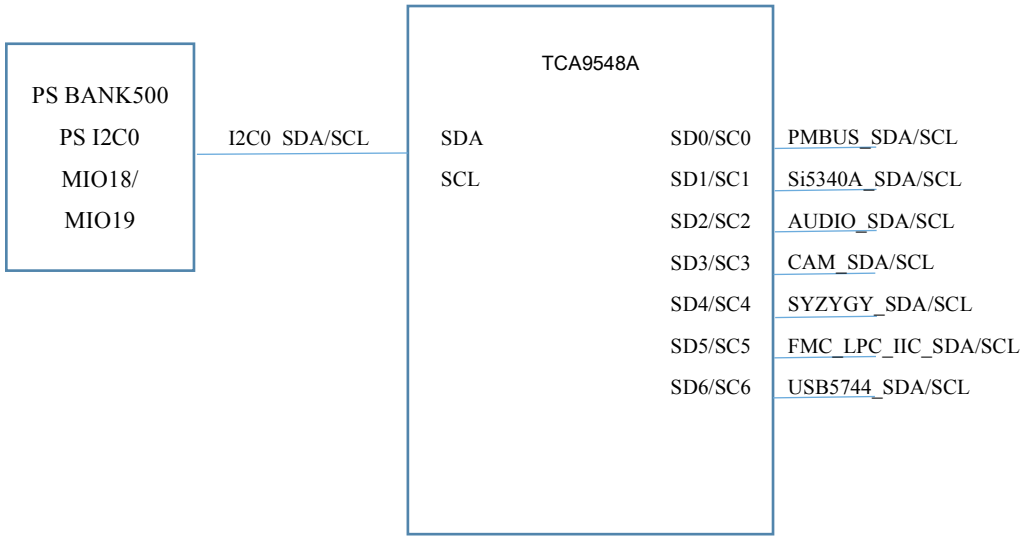


Figure 3-4 I2C0 Bus Topology

I2C Mux(Addr 0x75) Port	I2C BUS Device	I2C Address
0	PMBUS	attached device dependent
1	Si5340A Clock	0x74
2	AUDIO	0x6E
3	CAM MIPI	attached device dependent
4	SYZYGY	Port A(0x32) Port B(0x3D)
5	FMC_LPC	attached device dependent
6	USB5744	attached device dependent

PS Composite USB

The PYNQ-ZU board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver to support a USB connection to the host computer (see Figure 3-5). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard.

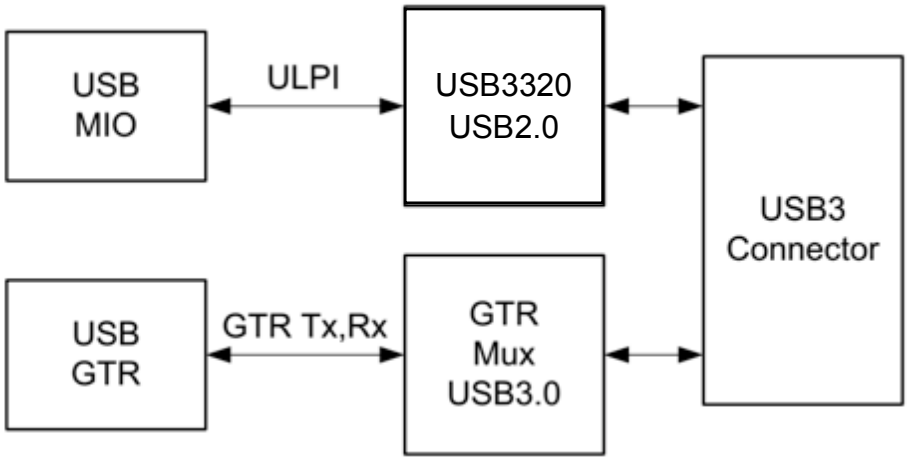


Figure 3-5 USB Interface

The USB3320 is clocked by a 24 MHz crystal.

The interface to the USB3320 PHY is implemented through the IP in the XCZU5EG MPSoC Processor System (PS).

USB 2.0 ULPI Upstream Connections to the XCZU5EG MPSoC

XCZU5EG Pin	Net Name	USB3320	
		Pin Number	Pin Name
AB21 & P16	USB_RST_B	27	RESET_B
F18	MIO58_USB0_STP	29	STP
D16	MIO53_USB0_DIR	31	DIR
G18	MIO52_USB0_CLK	1	CLKOUT
B16	MIO55_USB0_NXT	2	NXT
C16	MIO56_USB0_DATA0	3	DATA0
A16	MIO57_USB0_DATA1	4	DATA1
F17	MIO54_USB0_DATA2	5	DATA2
E17	MIO59_USB0_DATA3	6	DATA3
C17	MIO60_USB0_DATA4	7	DATA4
D17	MIO61_USB0_DATA5	9	DATA5
A17	MIO62_USB0_DATA6	10	DATA6
E18	MIO63_USB0_DATA7	13	DATA7

USB3.0 GTR

XCZU5EG Pin	Net Name	USB Connect Name
C25	GTR_LANE2_TX_P	SSTX+
C26	GTR_LANE2_TX_N	SSTX-
B27	GTR_LANE2_RX_P	SSRX+
B28	GTR_LANE2_RX_N	SSRX-

PS USB 3.0 Hub

The PYNQ-ZU board uses a Microchip USB5744 USB Controller Smart Hub to support a USB Hub to the slave device(see Figure 3-6). Microchip USB5744 4-Port SuperSpeed/High-speed USB Controller Smart Hub provides low-power, OEM configurability, and advanced features for embedded USB applications. All enabled downstream ports are supported through 5Gbps SuperSpeed (SS), 480Mbps Hi-Speed (HS), 12Mbps Full-Speed (FS), and 1.5Mbps Low-Speed (LS) USB downstream devices. USB 3.0 Hub is shown in Figure 3-7.

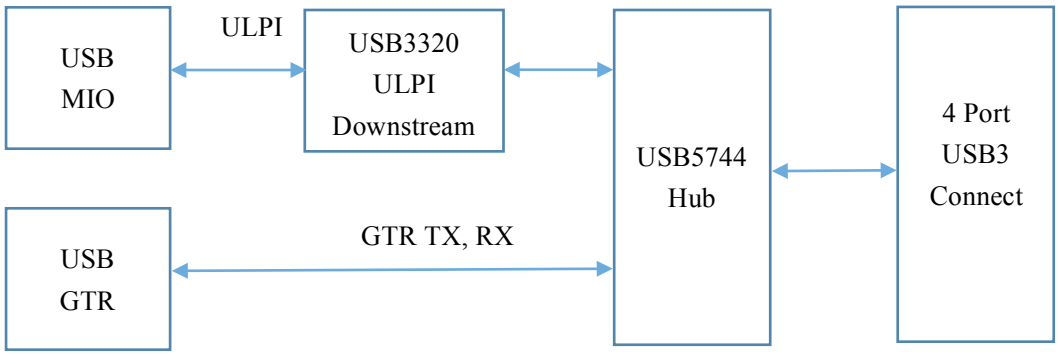


Figure 3-6 USB Hub

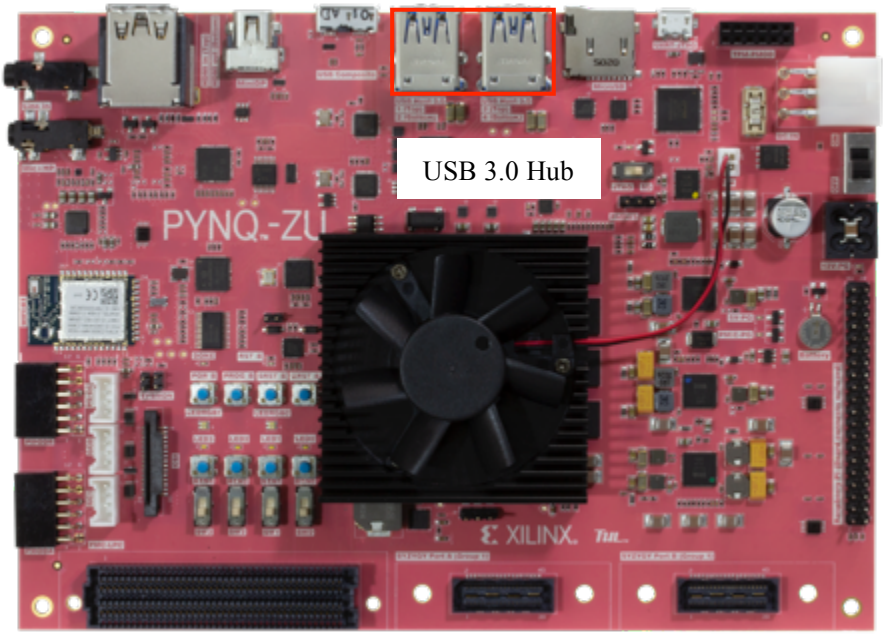


Figure 3-7

USB 2.0 ULPI Downstream Connections to the XCZU5EG MPSoC

XCZU5EG Pin	Net Name	USB3320	
		Pin Number	Pin Name
AB21 & P16	USB_RST_B	27	RESET_B
C19	MIO70_USB1_STP	29	STP
A18	MIO65_USB1_DIR	31	DIR
E19	MIO64_USB1_CLK	1	CLKOUT
B18	MIO67_USB1_NXT	2	NXT
C18	MIO68_USB1_DATA0	3	DATA0
D19	MIO69_USB1_DATA1	4	DATA1
G19	MIO66_USB1_DATA2	5	DATA2
B19	MIO71_USB1_DATA3	6	DATA3
G20	MIO72_USB0_DATA4	7	DATA4
G21	MIO73_USB0_DATA5	9	DATA5
D20	MIO74_USB0_DATA6	10	DATA6
A19	MIO75_USB0_DATA7	13	DATA7

USB3.0 GTR

XCZU5EG Pin	Net Name	USB5744
B23	GTR_LANE3_TX_P	USB3DM_TXUP
B24	GTR_LANE3_TX_N	USB3DP_TXUP
A25	GTR_LANE3_RX_P	USB3DM_RXUP
A26	GTR_LANE3_RX_N	USB3DP_RXUP

PS Mini Display Port

The PYNQ-ZU contain a Mini Display Port. The Zynq UltraScale+ MPSoC provides a VESA DisplayPort 1.2 source-only controller that supports up to two lanes of main link data at rates of 1.62 Gb/s, 2.70 Gb/s, or 5.40 Gb/s. The DisplayPort standard defines an auxiliary channel that uses LVDS signaling at a 1 Mb/s data rate, which is translated from single-ended MIO signals to the differential DisplayPort AUX channel.

Wifi+BT

The PYNQ-ZU contain a Wifi + BT Module ATWILC3000-MR110CA. The ATWILC3000-MR110CA module is an IEEE 802.11 b/g/n RF/Baseband/Medium Access Control(MAC) link controller and Bluetooth 4.0 compliant module, optimized for low power mobile applications.This module supports single stream 1x1 IEEE 802.11n mode providing up to 72 Mbps PHY rate. TheATWILC3000-MR110CA module features small form factor when integrating Power Amplifier (PA), LowNoise Amplifier (LNA), Transmit/Receive switch, Power Management, and chip Antenna. This module offers very low power consumption while simultaneously providing high performance.

MIO	Net Name	ATWILC3000 Pin Name
46	MIO46_SD_DAT0	SD_DAT0
47	MIO47_SD_DAT1	SD_DAT1
48	MIO48_SD_DAT2	SD_DAT2
49	MIO49_SD_DAT3	SD_DAT3
50	MIO50_SD_CMD	SD_CMD
51	MIO51_SD_CLK	SD_SCK
9	MIO9_UART1_RXD	BT_TXD
8	MIO8_UART1_TXD	BT_RXD
10	MIO10_BT_RTS	BT_RTS
11	MIO11_BT_CTS	BT_CTS
45	MIO45_WIFI_IRQN	IRQN
4	MIO4_WIFI_CHIP_EN	CHIP_EN
5	MIO5_WIFI_RESET_N	RESET_N

Wifi+BT block diagram is shown in Figure 3-8.

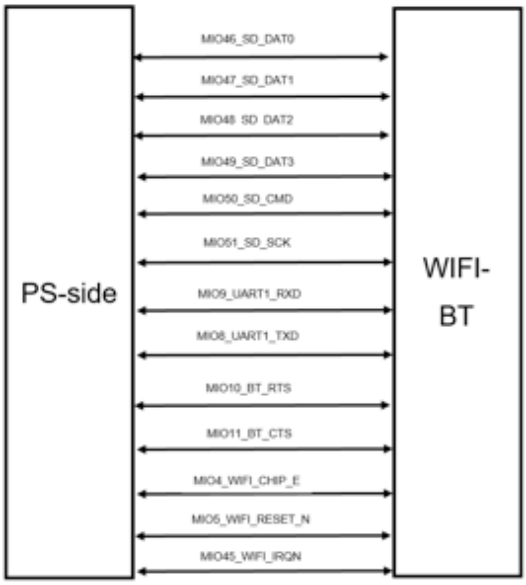


Figure 3-8 Wifi+BT Diagram

PL Connected Peripherals

HDMI Video TX

The PYNQ-ZU board provides a (HDMI™)(see Figure 3-9) video output. The HDMI output is provided on a upper port of the dual-stacked HDMI receptacle. The SN65DP159RGZ device is a dual mode DisplayPort to (TMDS) retimer supporting digital video interface (DVI) 1.0 and HDMI 1.4b and 2.0 output signals. The SN65DP159RGZ device supports the dual mode standard version 1.1 type 1 and type 2 through the DDC link or AUX channel. The HDMI video transmit block diagram is shown in Figure 3-10.

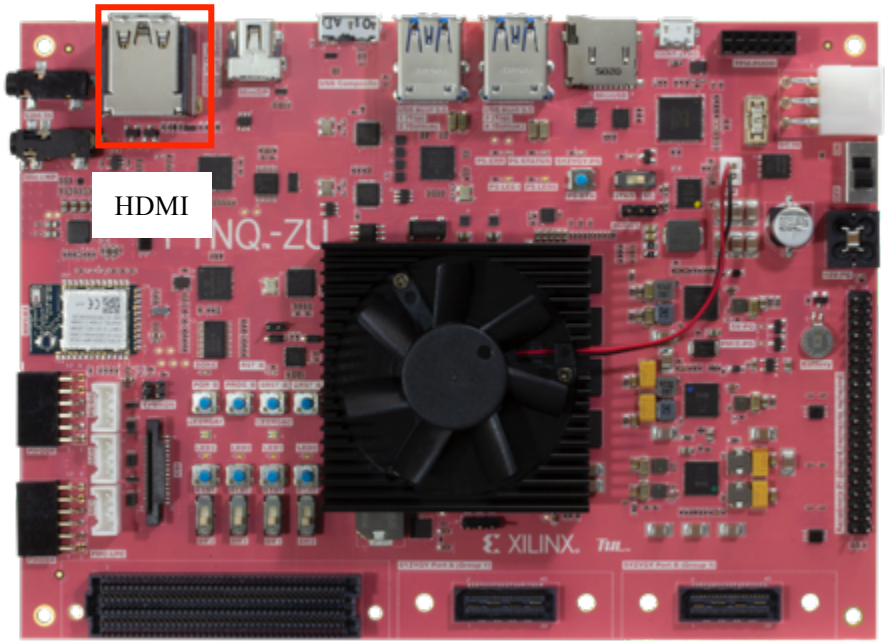


Figure 3-9

HDMI Video RX

The PYNQ-ZU board accepts HDMI video input the dual-stacked HDMI lower port.

The PYNQ-ZU HDMI RX interface supports up to 4K 60-Hz resolutions. See the Xilinx HDMI IP documentation for more details about resolutions, color spaces, and optional HDCP features supported by the Zynq® UltraScale+™ device.
The HDMI video transmit block diagram is shown in Figure 3-10.

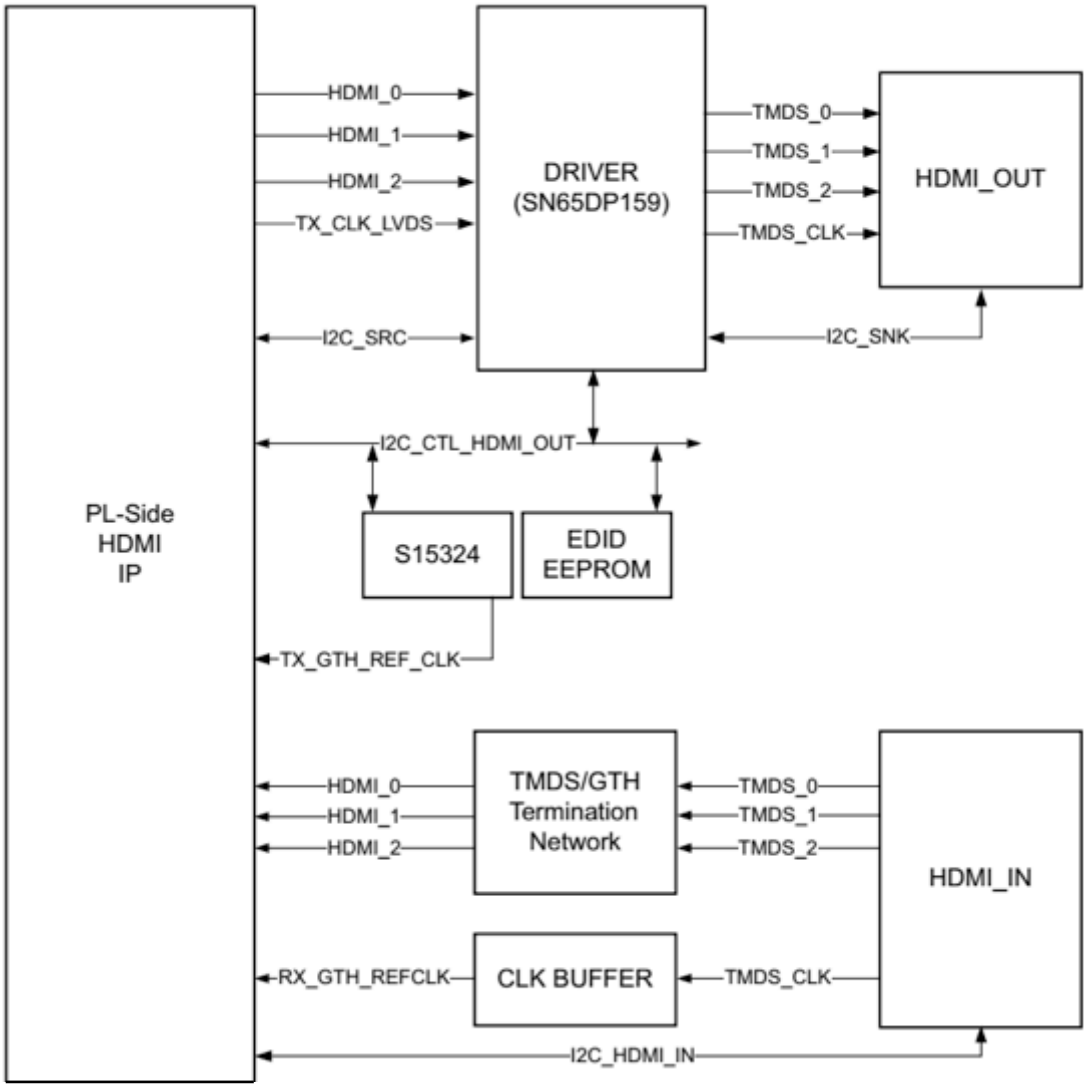


Figure 3-10 HDMI TX /RX Diagram

XCZU5EG Pin	Schematic Net Name	Connect Comonent	
		Pin Name	Device
W4	HDMI_TX_P0	IN_DP0	SN65DP159
W3	HDMI_TX_N0	IN_DN0	
U4	HDMI_TX_P1	IN_DP1	
U3	HDMI_TX_N1	IN_DN1	
R4	HDMI_TX_P2	IN_DP2	
R3	HDMI_TX_N2	IN_DN2	
AB6	HDMI_TX_LVDS_OUT_P	IN_CLKP	
AC6	HDMI_TX_LVDS_OUT_N	IN_CLKN	
A14	HDMI_TX_SRC_SCL	SCL_SRC	
B14	HDMI_TX_SRC_SDA	SDA_SRC	
A13	HDMI_TX_EN	OE	
A15	HDMI_CTL_SCL	SCL_CTL	
B15	HDMI_CTL_SDA	SDA_CTL	
B13	HDMI_TX_CEC	CEC_A	TPD12S016
C14	HDMI_TX_HPD	HPD_A	
E14	HDMI_TX_LS_OE	LS_OE	
D14	HDMI_TX_CT_HPD	CT_HPD	
E13	HDMI_SI5324_RST	RST_B	Si5324C
B15	HDMI_CTL_SDA	SDA/SDIO	
A15	HDMI_CTL_SCL	SCL	
F13	HDMI_SI5324_LOL	LOL	
G13	HDMI_SI5324_INT_ALM	INT_C1B	
H4	HDMI_REC_CLOCK_P	CKIN1_P	
H3	HDMI_REC_CLOCK_N	CKIN1_N	
FMC-D4	FMC_LPC_GBTCLK0_M2C_P	CKIN2_P	
FMC-D5	FMC_LPC_GBTCLK0_M2C_N	CKIN2_N	
Y6	HDMI_SI5324_OUT_P	CKOUT1_P	
Y5	HDMI_SI5324_OUT_N	CKOUT1_N	
Y2	HDMI_RX_P0	OUT_DP0	TMDS181I
Y1	HDMI_RX_N0	OUT_DN0	
V2	HDMI_RX_P1	OUT_DP1	
V1	HDMI_RX_N1	OUT_DN1	
T2	HDMI_RX_P2	OUT_DP2	
T1	HDMI_RX_N2	OUT_DN2	
V6	HDMI_RX_CLK_P	OUT_CLKP	
V5	HDMI_RX_CLK_N	OUT_CLKN	
L14	HDMI_RX_HPD	HPD_SNK	
B15	HDMI_CTL_SDA	SCL_CTL	
A15	HDMI_CTL_SCL	SDA_CTL	
L13	HDMI_RX_PWR_DET		

D15	HDMI_RX_SCL	D1-	TPD4E05U06DQA
C13	HDMI_RX_SDA	D2+	
	HDMI_RX_HPD_OUT	D2-	

AUDIO

The PYNQ-ZU provides MIC+HP (see Figure 3-11) and Line IN Connector. The ADAU1761 is a low power, stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control. SYSTEM BLOCK DIAGRAM as show in Figure 3-12.

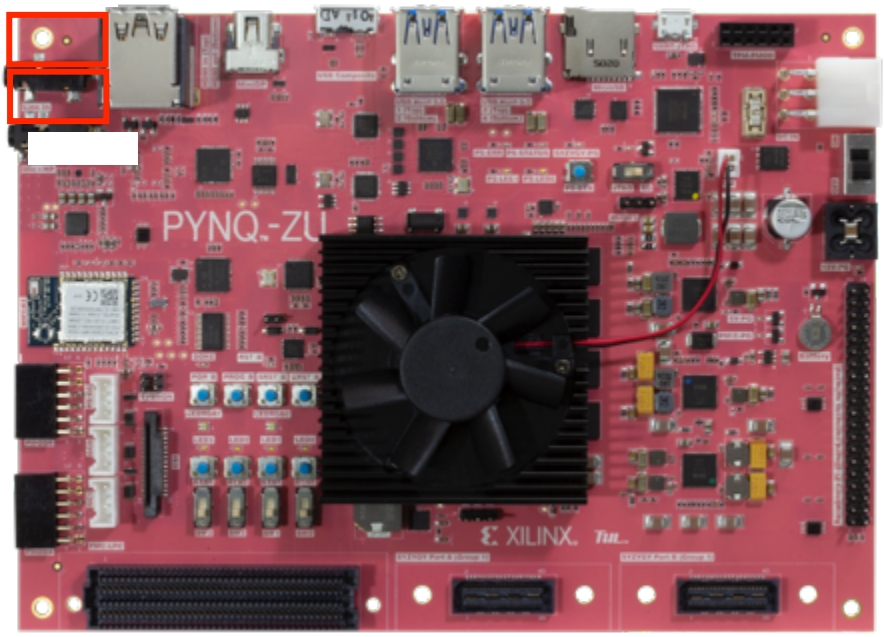


Figure 3-11

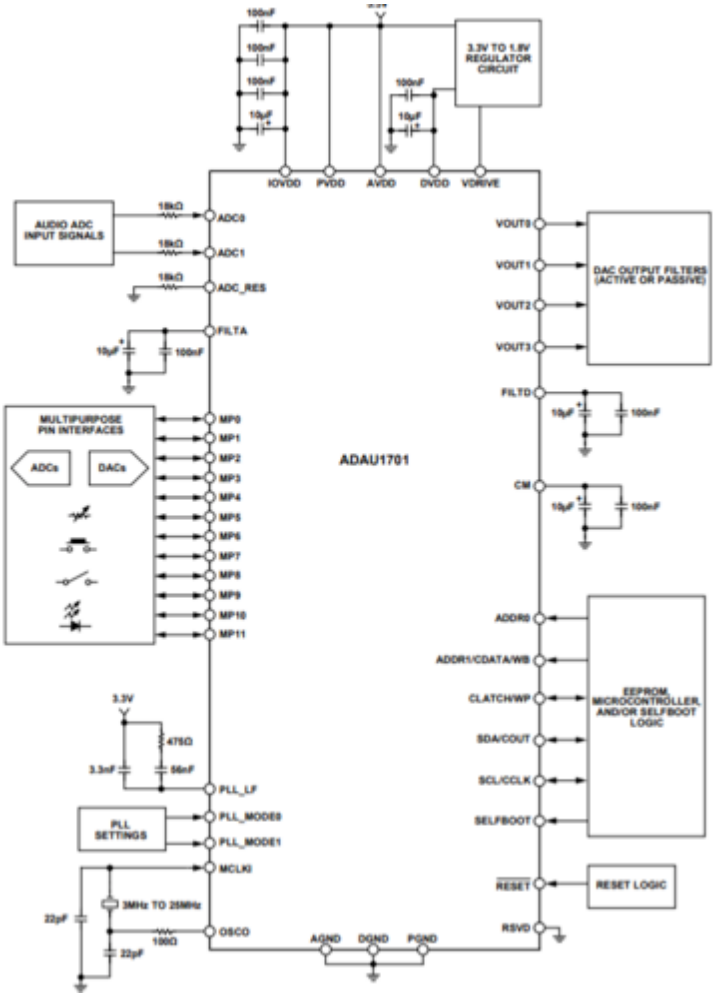


Figure 3-12 System Block Diagram

Audio & Jack

XCZU5EG Pin	Net Name	USB5744
K14	AUDIO_DOUT	ADC_SDATA/GPIO1
H13	AUDIO_DIN	DAC_SDATA/GPIO0
E15	AUDIO_BCLK	BCLK/GPIO2
F15	AUDIO_WCLK	LRCLK/GPIO3
H14	AUDIO_ADR0	ADR0/CLATCH
G14	AUDIO_ADR1	ADR1/CDATA
PS_MIO18	AUDIO_SDA	SDA/COUT
PS_MIO19	AUDIO_SCL	SCK/CCLK
G15	AUDIO_MCLK	MCLK

User I/O

The PYNQ-ZU board provides these general purpose I/O capabilities, as shown in Figure 3-13.

- Four user LEDs
- Four user DIP switches
- Four user push buttons
- Two user RGBLEDs

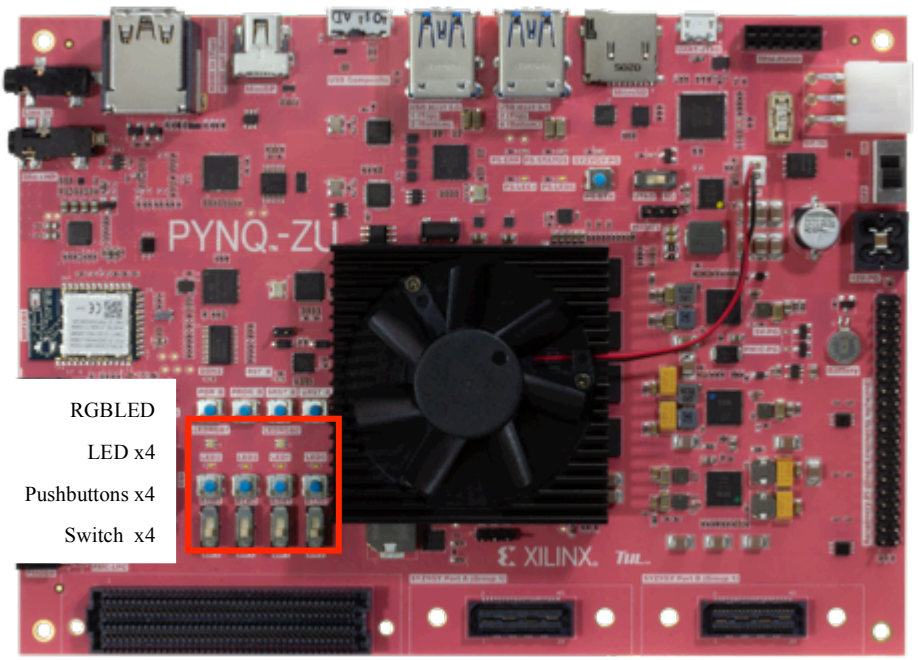


Figure 3-13

XCZU5EG Pin	Net Name	User I/O
A9	LED_B0	LEDRGB0
A5	LED_G0	
A4	LED_R0	
A8	LED_B1	LEDRGB1
B9	LED_G1	
B6	LED_R1	
B5	LED0	LED
A6	LED1	
B8	LED2	
A7	LED3	
AA12	SW0	DIP switches
Y12	SW1	
W11	SW2	
W12	SW3	
AH14	BTN0	Push buttons
AG14	BTN1	
AE14	BTN2	
AE15	BTN3	

PYNQ-ZU provides peripheral IO, as shown in Figure 3-14

- MIPI CSI
- Pmods
- FMC LPC
- SYZYGY Standard Ports
- Grove Interface ports
- Raspberry PI GPIO
- TPM PMOD
- External Analog Inputs

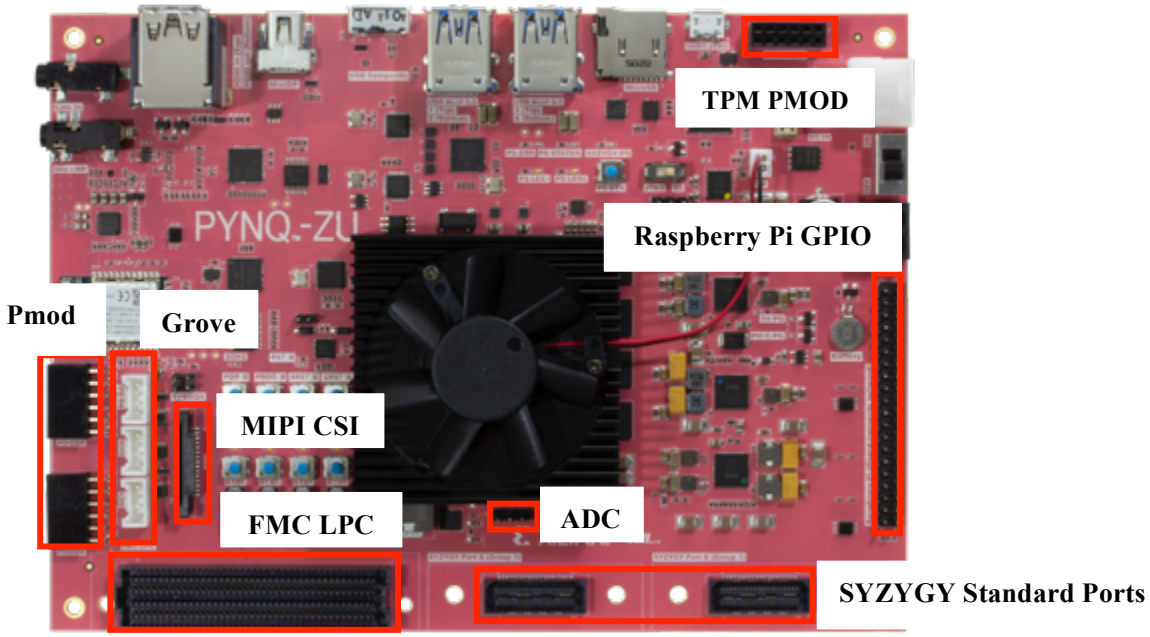


Figure 3-14 Extended IO

MIPI CSI

The MIPI CSI port included on the PYNQ-ZU are 30-pin. CSI (Camera Serial Interface) is the Interface standard specified by the Camera Working group under the MIPI Alliance

XCZU5EG PIN	Connector Pin Number(J6)	Net Name
	1	GND
	2	GND
D5	3	MIPI_LANE_N0
	4	MIPI_LANE_N0
E5	5	MIPI_LANE_P0
	6	MIPI_LANE_P0
	7	GND
	8	GND
F6	9	MIPI_LANE_N1
	10	MIPI_LANE_N1
G6	11	MIPI_LANE_P1
	12	MIPI_LANE_P1
	13	GND
	14	GND
D6	15	MIPI_CLK_N
	16	MIPI_CLK_N
D7	17	MIPI_CLK_P
	18	MIPI_CLK_P
	19	GND
	20	GND
AH7	21	CAM_GPIO
	22	CAM_GPIO
AH8	23	CAM_CLK
	24	CAM_CLK
MIO18	25	CAM__SCL
	26	CAM__SCL
MIO19	27	CAM_SDA
	28	CAM_SDA
	29	VCC3V3
	30	VCC3V3

PMOD

The PYNQ-ZU provide 2 Pmod ports. The ports are 2×6, right-angle, 100-mil spaced female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod port provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight 3.3V compliant logic signals, as shown in Figure 3-15.

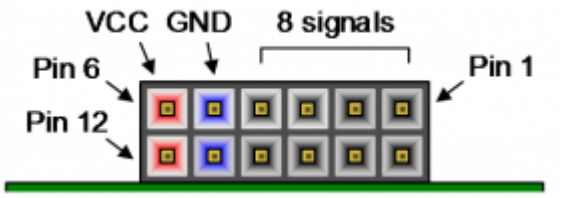


Figure 3-15 Pmod Port

PmodA Diagram

XCZU5EG PIN	Net Name
T8	PMOD0_0
R8	PMOD0_1
V8	PMOD0_2
U8	PMOD0_3
V9	PMOD0_4
U9	PMOD0_5
Y8	PMOD0_6
W8	PMOD0_7

PmodB Diagram

XCZU5EG PIN	Net Name
F5	PMOD1_0
G5	PMOD1_1
E3	PMOD1_2
E4	PMOD1_3
F3	PMOD1_4
G3	PMOD1_5
E2	PMOD1_6
F2	PMOD1_7

FMC LPC

The PYNQ-ZU board supports the VITA 57.1 FPGA Mezzanine Card (FMC) specification by providing subset implementations of low pin count (LPC) connectors at FMC-LPC. This connector uses a 10 x 40 form factor that is partially populated with 160 pins. The connector is keyed so that a the mezzanine card faces away from the PYNQ-ZU board when connected.

Connector Type:

• Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector.

LPC Connector , FMC-LPC to XCZU5EG

FMC-LPC	Net Name	I/O Standard	XCZU5EG PIN	FMC-LPC	Net Name	I/O Standard	XCZU5EG PIN
C2	FMC_LPC_DP0_C2M_P		N4	D1	VADJ_FMC_PGOOD		
C3	FMC_LPC_DP0_C2M_N		N3	D4	FMC_LPC_GBTCLK0_M2C_P		
C6	FMC_LPC_DP0_M2C_P		P2	D5	FMC_LPC_GBTCLK0_M2C_N		
C7	FMC_LPC_DP0_M2C_N		P1	D8	FMC_LPC_LA01_CC_P		P7
C10	FMC_LPC_LA06_P		J7	D9	FMC_LPC_LA01_CC_N		P6
C11	FMC_LPC_LA06_N		H7	D11	FMC_LPC_LA05_P		J1
C14	FMC_LPC_LA10_P		N7	D12	FMC_LPC_LA05_N		H1
C15	FMC_LPC_LA10_N		N6	D14	FMC_LPC_LA09_P		L1
C18	FMC_LPC_LA14_P		R7	D15	FMC_LPC_LA09_N		K1
C19	FMC_LPC_LA14_N		T7	D17	FMC_LPC_LA13_P		R6
C22	FMC_LPC_LA18_CC_P		AD2	D18	FMC_LPC_LA13_N		T6
C23	FMC_LPC_LA18_CC_N		AD1	D20	FMC_LPC_LA17_CC_P		AC4
C26	FMC_LPC_LA27_P		AE3	D21	FMC_LPC_LA17_CC_N		AC3
C27	FMC_LPC_LA27_N		AF3	D23	FMC_LPC_LA23_P		AC9
C30	FMC_LPC_IIC_SCL		MIO18	D24	FMC_LPC_LA23_N		AD9
C31	FMC_LPC_IIC_SDA		M19	D26	FMC_LPC_LA26_P		AF1
C34	NC			D27	FMC_LPC_LA26_N		AG1
C35	FMC_12V			D29	FT2232H_JTAG_TCK		
C37	FMC_12V			D30	FPGA_TDO_FMC_TD		
C39	FMC_3V3			D31	FMC_TDO		
				D32	FMC_3V3		
				D33	FT2232H_JTAG_TMS		
				D34	NC		
				D35	NC		
				D36	FMC_3V3		
				D38	FMC_3V3		
				D40	FMC_3V3		

FMC-LPC	Net Name	I/O Standard	XCZU5EG PIN	FMC-LPC	Net Name	I/O Standard	XCZU5EG PIN
G2	FMC_LPC_CLK1_M2C_P		AE5	H1	FMC_LPC_VREF_A_M2C		
G3	FMC_LPC_CLK1_M2C_N		AF5	H2	FMC_LPC_PRSNT_M2C_B		
G6	FMC_LPC_LA00_CC_P		L7	H4	FMC_LPC_CLK0_M2C_P		L3
G7	FMC_LPC_LA00_CC_N		L6	H5	FMC_LPC_CLK0_M2C_N		L2
G9	FMC_LPC_LA03_P		K9	H7	FMC_LPC_LA02_P		K8
G10	FMC_LPC_LA03_N		J9	H8	FMC_LPC_LA02_N		K7
G12	FMC_LPC_LA08_P		J5	H10	FMC_LPC_LA04_P		H9
G13	FMC_LPC_LA08_N		J4	H11	FMC_LPC_LA04_N		H8
G15	FMC_LPC_LA12_P		M6	H13	FMC_LPC_LA07_P		J6
G16	FMC_LPC_LA12_N		L5	H14	FMC_LPC_LA07_N		H6
G18	FMC_LPC_LA16_P		M8	H16	FMC_LPC_LA11_P		K2
G19	FMC_LPC_LA16_N		L8	H17	FMC_LPC_LA11_N		J2
G21	FMC_LPC_LA20_P		AB4	H19	FMC_LPC_LA15_P		N9
G22	FMC_LPC_LA20_N		AB3	H20	FMC_LPC_LA15_N		N8
G24	FMC_LPC_LA22_P		AB1	H22	FMC_LPC_LA19_P		AB2
G25	FMC_LPC_LA22_N		AC1	H23	FMC_LPC_LA19_N		AC2
G27	FMC_LPC_LA25_P		AH2	H25	FMC_LPC_LA21_P		AE2
G28	FMC_LPC_LA25_N		AH1	H26	FMC_LPC_LA21_N		AF2
G30	FMC_LPC_LA29_P		AG4	H28	FMC_LPC_LA24_P		AG3
G31	FMC_LPC_LA29_N		AH4	H29	FMC_LPC_LA24_N		AH3
G33	FMC_LPC_LA31_P		AG9	H31	FMC_LPC_LA28_P		AG6
G34	FMC_LPC_LA31_N		AH9	H32	FMC_LPC_LA28_N		AG5
G36	FMC_LPC_LA33_P		AD7	H34	FMC_LPC_LA30_P		AE9
G37	FMC_LPC_LA33_N		AE7	H35	FMC_LPC_LA30_N		AE8
G39	FMC_VADJ			H37	FMC_LPC_LA32_P		AF8
				H38	FMC_LPC_LA32_N		AG8
				H40	FMC_VADJ		

Dual SYZYGY Standard Ports

The PYNQ-ZU use the SYZYGY Standard interface to communicate with installed SYZYGY pods. 2 SYZYGY standard interfaces available on the board. Standard Peripheral as shown in Figure 3-16

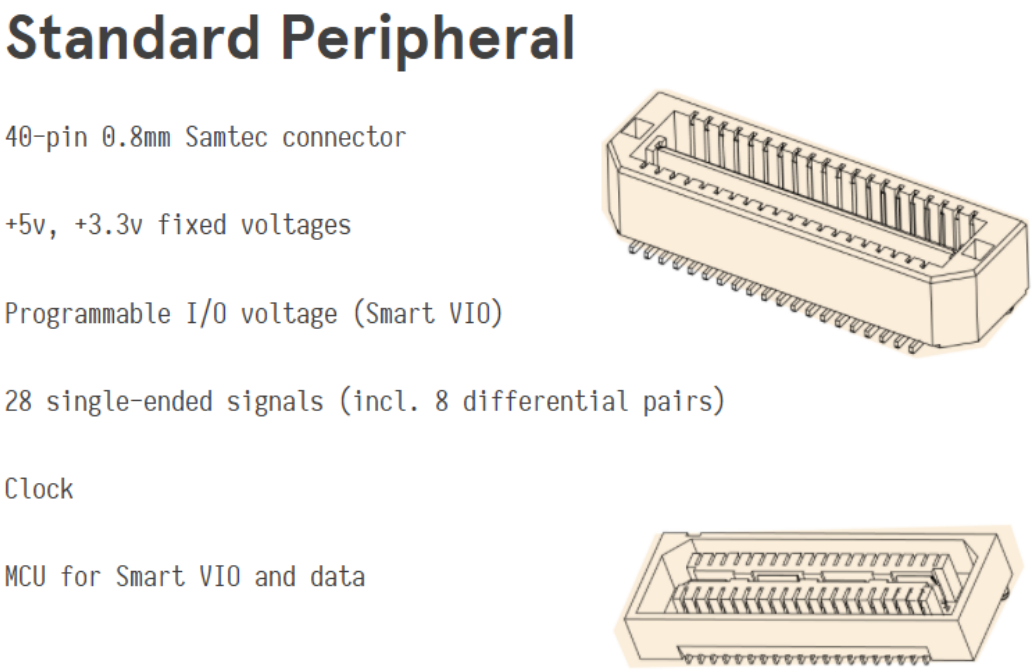


Figure 3-16 SYZYGY Interface Connectors

SYZYGY Port A

SYZYGY Port A Number	SYZYGY Port A name	Net Name	I/O Standard	XCZU5EG PIN	SYZYGY Port A Number	SYZYGY Port A name	Net Name	I/O Standard	XCZU5EG PIN
1	SCL	SYZYGY_SCL		MIO_18	6	S1_D1P	SYZYGY1_DP1		AH12
3	SDA	SYZYGY_SDA		MIO_19	8	S3_D1N	SYZYGY1_DN1		AH11
5	S0_D0P	SYZYGY1_DP0		AE10	10	S5_D3P	SYZYGY1_DP3		AG10
7	S2_D0N	SYZYGY1_DN0		AF10	12	S7_D3N	SYZYGY1_DN3		AH10
9	S4_D2P	SYZYGY1_DP2		AF11	14	S9_D5P	SYZYGY1_DP5		AE13
11	S6_D2N	SYZYGY1_DN2		AG11	16	S11_D5N	SYZYGY1_DN5		AF13
13	S8_D4P	SYZYGY1_DP4		AD15	18	S13_D7P	SYZYGY1_DP7		AG13
15	S10_D4N	SYZYGY1_DN4		AD14	20	S15_D7N	SYZYGY1_DN7		AH13
17	S12_D6P	SYZYGY1_DP6		AC14	22	S17	SYZYGY1_S17		AA11
19	S14_D6N	SYZYGY1_DN6		AC13	24	S19	SYZYGY1_S19		AD11
21	S16	SYZYGY1_S16		W10	26	S21	SYZYGY1_S21		AC11
23	S18	SYZYGY1_S18		Y9	28	S23	SYZYGY1_S23		AD10
25	S20	SYZYGY1_S20		Y10	30	S25	SYZYGY1_S25		AB11
27	S22	SYZYGY1_S22		AA8	32	S27	SYZYGY1_S27		AB10
29	S24	SYZYGY1_S24		AA10	34	C2P_CLKP	SYZYGY1_C2P_CLKP		AE12
31	S26	SYZYGY1_S26		AB9	36	C2P_CLKN	SYZYGY1_C2P_CLKN		AF12
33	P2C_CLKP	SYZYGY1_P2C_CLKP		AC12					
35	P2C_CLKN	SYZYGY1_P2C_CLKN		AD12					

SYZYGY Port B

SYZYGY Port A Number	SYZYGY Port A name	Net Name	I/O Standard	XCZU5EG PIN	SYZYGY Port A Number	SYZYGY Port A name	Net Name	I/O Standard	XCZU5EG PIN
1	SCL	SYZYGY_SCL		MIO_18	6	S1_D1P	SYZYGY2_DP1		J12
3	SDA	SYZYGY_SDA		MIO_19	8	S3_D1N	SYZYGY2_DN1		H12
5	S0_D0P	SYZYGY2_DP0		J11	10	S5_D3P	SYZYGY2_DP3		K13
7	S2_D0N	SYZYGY2_DN0		J10	12	S7_D3N	SYZYGY2_DN3		K12
9	S4_D2P	SYZYGY2_DP2		H11	14	S9_D5P	SYZYGY2_DP5		AA13
11	S6_D2N	SYZYGY2_DN2		G10	16	S11_D5N	SYZYGY2_DN5		AB13
13	S8_D4P	SYZYGY2_DP4		Y14	18	S13_D7P	SYZYGY2_DP7		AB15
15	S10_D4N	SYZYGY2_DN4		Y13	20	S15_D7N	SYZYGY2_DN7		AB14
17	S12_D6P	SYZYGY2_DP6		W14	22	S17	SYZYGY2_S17		A11
19	S14_D6N	SYZYGY2_DN6		W13	24	S19	SYZYGY2_S19		C12
21	S16	SYZYGY2_S16		A12	26	S21	SYZYGY2_S21		B10
23	S18	SYZYGY2_S18		D12	28	S23	SYZYGY2_S23		C11
25	S20	SYZYGY2_S20		E12	30	S25	SYZYGY2_S25		B11
27	S22	SYZYGY2_S22		A10	32	S27	SYZYGY2_S27		E10
29	S24	SYZYGY2_S24		D11	34	C2P_CLKP	SYZYGY2_C2P_CLKP		G11
31	S26	SYZYGY2_S26		D10	36	C2P_CLKN	SYZYGY2_C2P_CLKN		F10
33	P2C_CLKP	SYZYGY2_P2C_CLKP		F12					
35	P2C_CLKN	SYZYGY2_P2C_CLKN		F11					

GROVE Interface

The PYNQ-ZU provide 3 Grove interfaces; one accessible from the PS side and two from the PL side

XCZU5EG PIN	Net Name	Port Name
PS_MIO0	PS_GROVE_IO1	PS_GC
PS_MIO1	PS_GROVE_IO2	
K5	PL_GROVE_IO1	GC0
P9	PL_GROVE_IO2	
AE4	PL_GROVE_IO3	GC1
AB5	PL_GROVE_IO4	

Raspberry Pi GPIOs

The PYNQ-ZU has a 40-pin Raspberry Pi connector with 28 pins connected to the XCZU5EG device.

G	D1	E7	C4	C2	A1	C8	G	D9	C9	B4	V	E9	G4	E8	G	E1	F1	D2	V
39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
C3	C6	C1	G	B1	G	C7	A2	B3	A3	G	G8	F8	G	G1	D4	F7	G	V	V

G	Ground
V	3.3V
V	5V
...	Raspberry Pi header pin number
...	ZU5EG Pin

FPGA pin	connector pin	connector pin	FPGA pin
	1	2	
D2	3	4	
F1	5	6	
E1	7	8	F7
	9	10	D4
E8	11	12	G1
G4	13	14	
E9	15	16	F8
	17	18	G8
B4	19	20	
C9	21	22	A3
D9	23	24	B3
	25	26	A2
C8	27	28	C7
A1	29	30	
C2	31	32	B1
C4	33	34	
E7	35	36	C1
D1	37	38	C6
	39	40	C3

TPM PMOD

The PYNQ-ZU contains a TPM PMOD port. **Trusted Platform Module** (**TPM**, also known as **ISO/IEC 11889**) is an international standard for a secure crypto processor, a dedicated microcontroller designed to secure hardware through integrated cryptographic keys.

XCZU5EG PIN	Port number
PS_MIO41	1
PS_MIO43	2
PS_MIO42	3
PS_MIO38	4
PS_MIO44	7
PS_MIO37	8
PS_MIO40	9
PS_MIO39	10

External Analog Inputs

The PYNQ-ZU provides an Analog Front End XADC block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Converter (ADC) and on-chip sensors. See the7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide for details on the capabilities of the analog front end. Figure 3-17 shows the XADC block diagram.

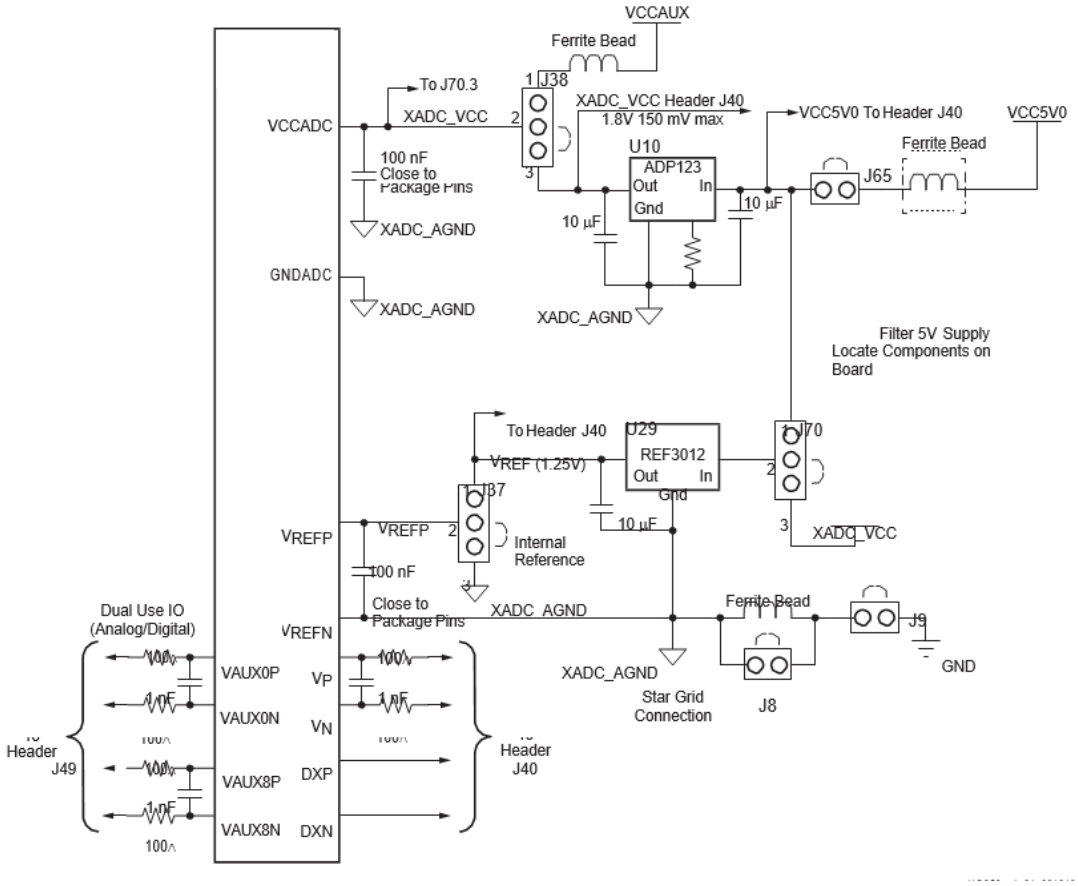


Figure 3-17 XADC Block Diagram.

XADC

XCZU5EG PIN	Net Name
AB7	AR_AN_P0
AB8	AR_AN_P1
AC7	AR_AN_N0
AC8	AR_AN_N1