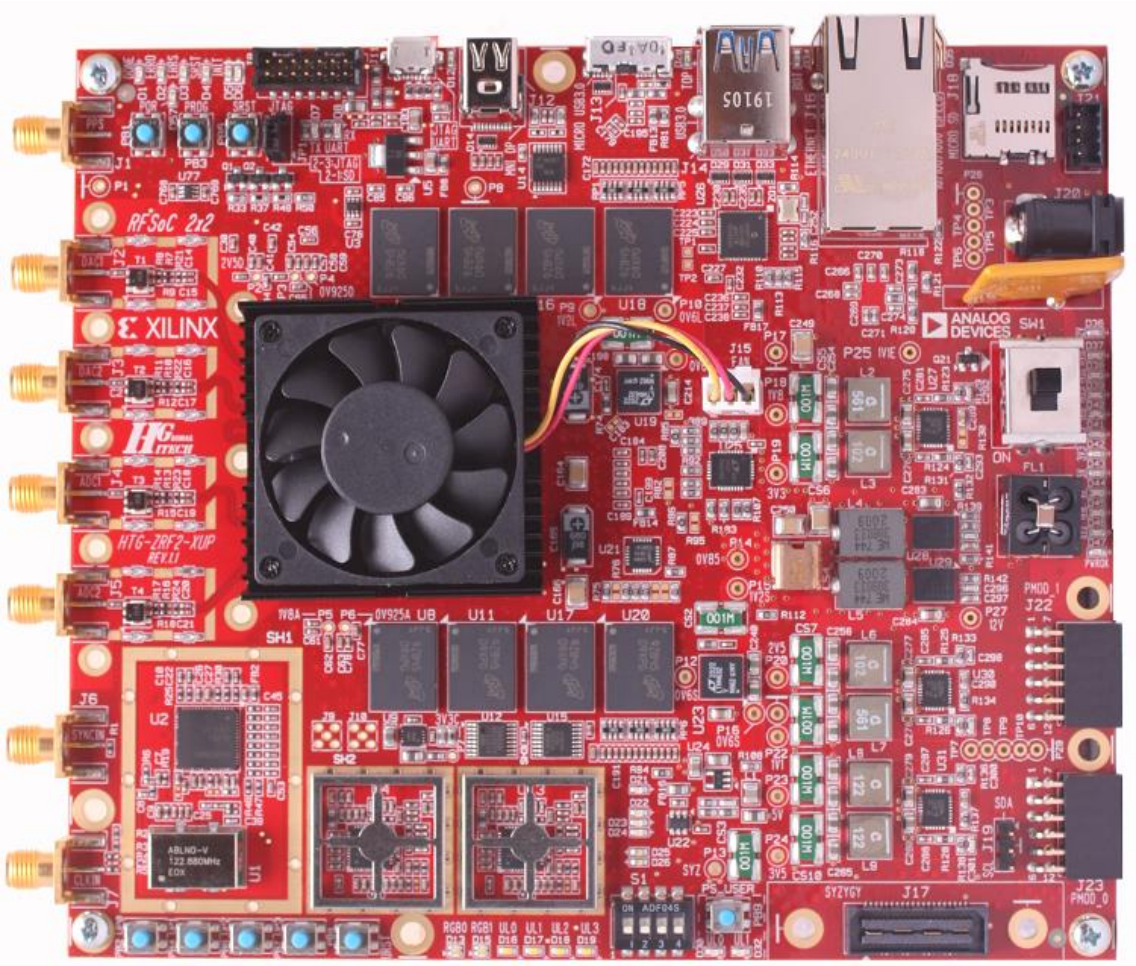
HiTech Global ZYNQ UltraScale+™ RFSoC Development Platform

RFSOC_2x2 User Manual

Version 1.0 January 2021



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Revision History

Date	Version	Notes
1/4/2021	1.0	

Table Of Contents

1.0) Overview	4
2.0) RFSOC 2X2Features	5
3.0) Banks Assignment, Block Diagram & Clocks Diagram	5
4.0) Main Clocks	9
5.0) DDR4 Memory	11
6.0) ADC and DAC Ports	18
7.0) USB Ports	22
8.0) SDIO Interface	23
9.0) 10/100/1000 Mbps Ethernet	23
10.0) Display Port	24
11.0) 1-PPS Interface	25
12.0) PMOD Ports	25
13.0) SYZYGY Port	26
14.0) LEDs, User Switch & Pushbuttons	27
15.0) Configuration	28

Tables

Table (1): Summary of supported ZYNQ RFSoC UltraScale+ FPGA Feature	5
Table (2): Main Clocks	11
Table (3): Summary of the Si5340 (U54) Clock Outputs	12
Table (4): DDR4 FPGA Pin Assignment (PL Side)	16
Table (5) DDR4 FPGA Pin Assignment (Processor Side)	19
Table (6): ADC Interface Pin Assignment	20
Table (7): DAC Interface Pin Assignment	20
Table (8): USB Interface Pin Assignment	25
Table (9): SDIO Port's FPGA Pin Assignment	25
Table (10): Ethernet Port's FPGA Pin Assignment	26
Table (11): Display Port's FPGA Pin Assignment	27
Table (12): 1-PPS Port's FPGA Pin Assignment	27
Table (13): PMOD Ports' FPGA Pin Assignment	28
Table (14): SYZYGY Voltage Configuration	28
Table (15): SYZYGY Port's FPGA Pin Assignment	29
Table (16): User Interface FPGA Pin Assignment	

Figures

Figure (1): FPGA I/O Bank Assignment	7
Figure (2): System Block Diagram	8
Figure (3): Clock Block Diagram	9
Figure (4): User Interface Ports/Controls	10
Figure (5): Si5340 Clock Generator Block Diagram	12
Figure (6): LMX2594 Block Diagram	13
Figure (7): ADC Ports – FPGA Interface	21
Figure (8): DAC Ports – FPGA Interface	22
Figure (9): ADC/DAC Clock Configuration	23

1.0) Overview

Populated with one Xilinx ZYNQ UltraScale+ RFSoC ZU28DR FPGA device, the RFSoC_2x2 platform provides access to large FPGA gate densities, two ADC/DAC ports, DDR4 memory, Gigabit Ethernet, USB , display port, PMOD and SYZYGY ports for variety of different programmable applications.

The RFSoC_2x2 platform is supported by two 12-bit ADC (4GSPS) and two14-bit DAC (6.4GSPS) ports. The ADC and DAC ports are supported through high-performance front panel micro Rf connectors. This board supports Multi-Tile Synchronization of the ADC/DAC channels.

Table (1) illustrates key features of the supported FPGAs by the RFSoC_2x2 platform.

	Device Name		ZU28DR	ZU48DR
RF Data Converter	12-bit RF-ADC w/DDC	# of ADCs	8	–
		Max Rate (GSPS)	4.096	–
	14-bit RF-ADC w/DDC	# of ADCs	–	8
		Max Rate (GSPS)	–	5.0
	14-bit RF-DAC w/DUC	# of DACs	8	8
		Max Rate (GSPS)	6.554	10.0
	SD-FEC		8	8
	Number of DDCs per RF-ADC[1]		1	1
	RF input Freq max. GHz			
	Decimation / Interpolation			16x, 20x, 24x,
Programmable Logic (PL)	System Logic Cells (K)		930	930
	CLB LUTs (K)		425	425
	Max. Dist. RAM (Mb)		13.0	13.0
	Total Block RAM (Mb)		38.0	38.0
	UltraRAM (Mb)		22.5	22.5
	DSP Slices		4,272	4,272
	GTY Transceivers		16	16
	PCIe® Gen3 x16		2	–
	PCIeGen3 x16/Gen4 x8 / CCIX[2]		–	2
	150G Interlaken		1	1
	100G Ethernet MAC/PCS w/RS-FEC		2	2
	System Monitor		1	1
	Speed Grades		-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI
Package Footprint	Package Dimensions		PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
G1517	40x40		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8

Table (1): Summary of supported ZYNQ RFSoC UltraScale+ FPGA Features

2.0) Hardware Features

►Xilinx Zynq UltraScale+ RFSoC ZU28DR (-2 speed grade)
►x2 ADC (12-bit , 4GSPS) ports (SMA connectors)
►x2 DAC (14-bit, 6.4GSPS) ports (SMA connectors)
►Support for Multi-Tile Synchronization of ADC/DAC channels
►Programmable ADC/DAC Clock Generator
►Independent DDR4 memory for the FPGA and processors (4GB components)
►x1 10/100/1000 Ethernet (RJ45) port (Processor Side)
►x1 MicroSD (Processor Side)
►x2 PMOD Port s(Programmable Logic Side)
►SYZYGY port (Programmable Logic Side)
►x1 Display Port (Processor Side)
►x2 (stacked) USB 3.0 Host (Processor Side)
►x1 USB 3.0 Slave (Processor Side)
►x1 USB 2.0 Slave (Processor Side)
►Programmable clocks
►x1 1PPS port (Programmable Logic Side)
►Current monitors
►Pushbuttons and LEDs
►FPGA JTAG header
►External synchronous clock port
►x2 SMA to SMA cables (12”)
►x1 wall power adapter (US. plug / 12V)

3.0) Banks Assignment, Block Diagram & Clocks Diagram

Figure (1) , (2), (3) and illustrate FPGA I/O bank assignment, system block, clocks and user interface ports/controls diagrams of the RFSoC_2x2 platform.

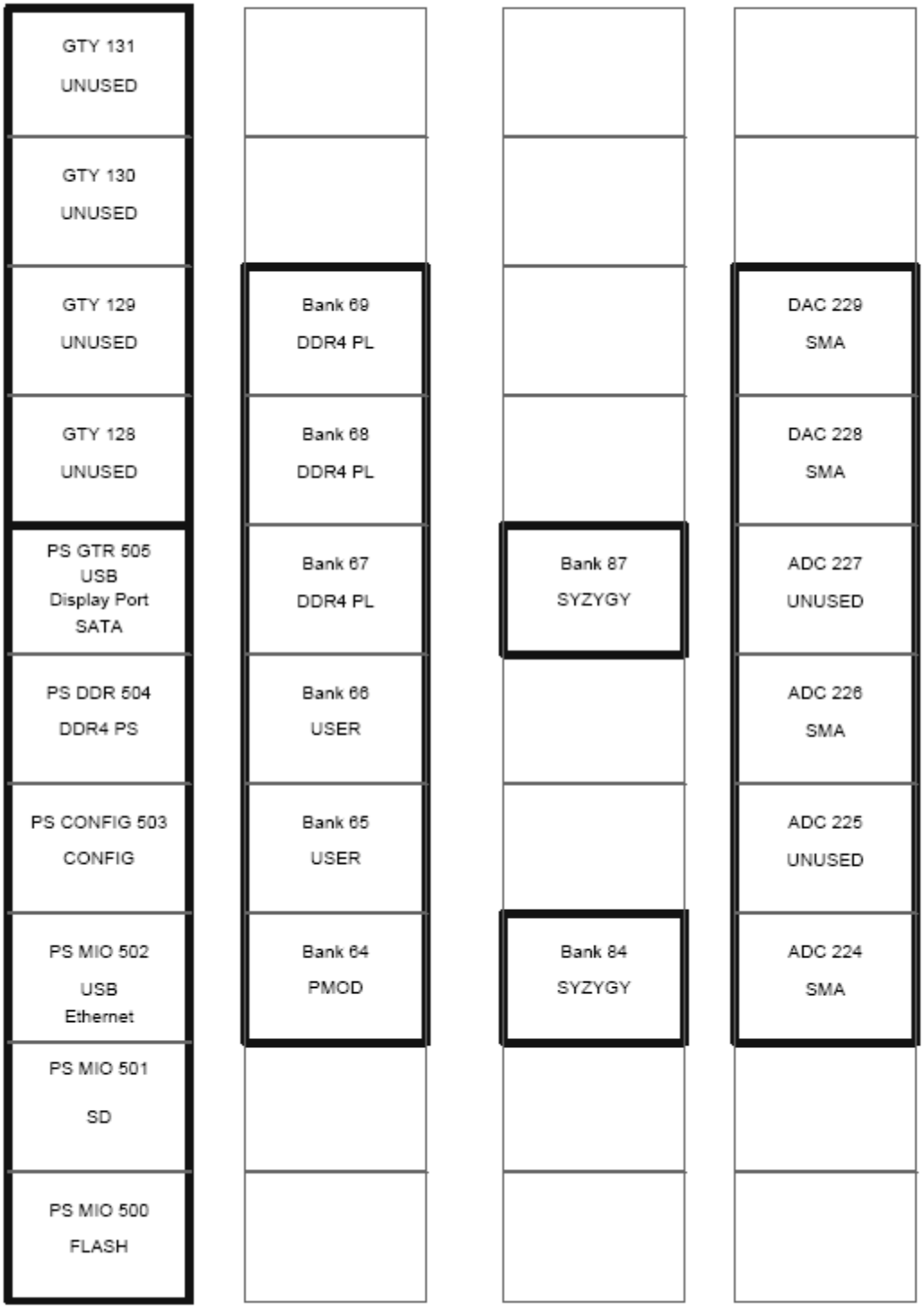

Figure (1): FPGA I/O Bank Assignment

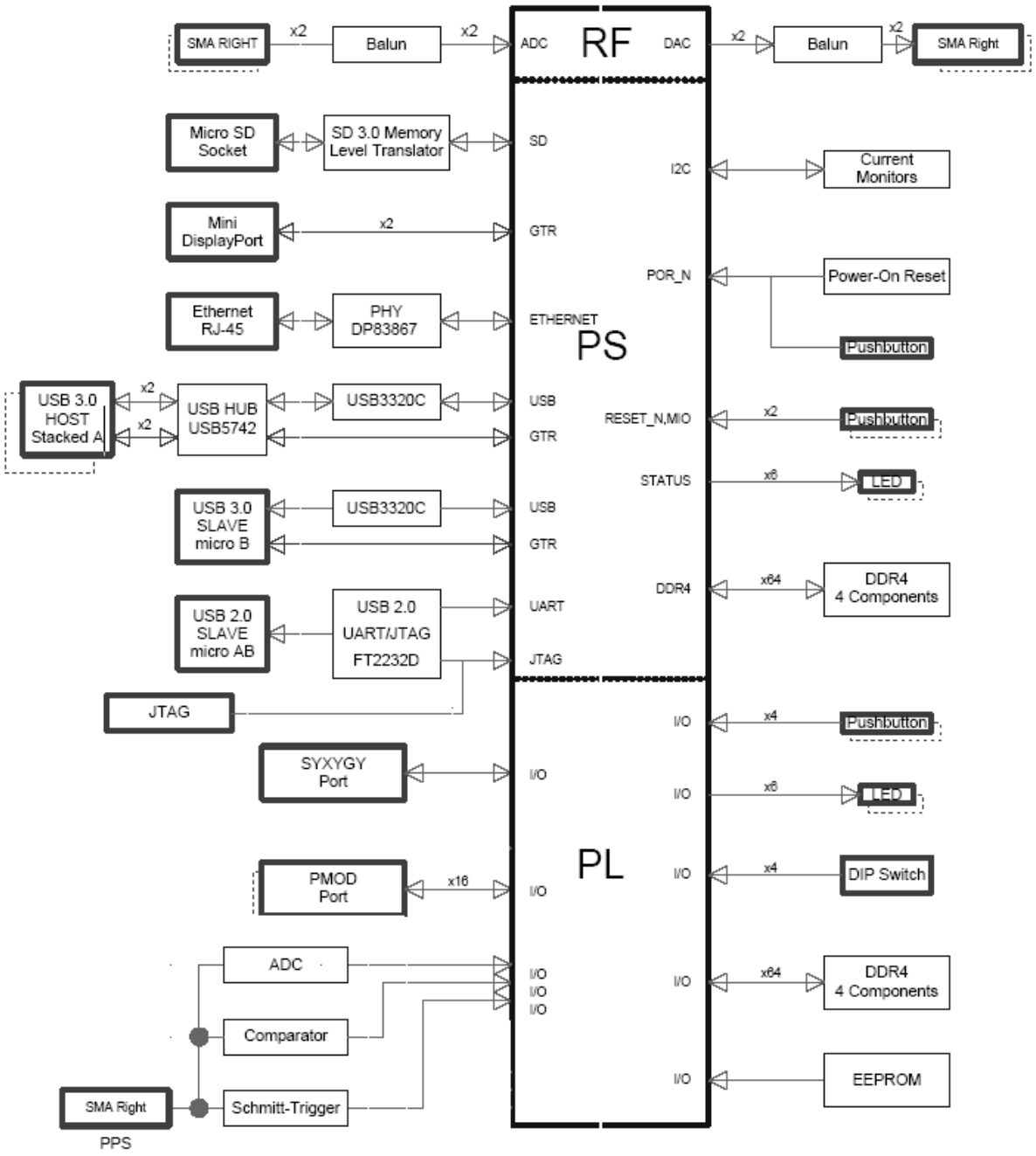

Figure (2): System Block Diagram

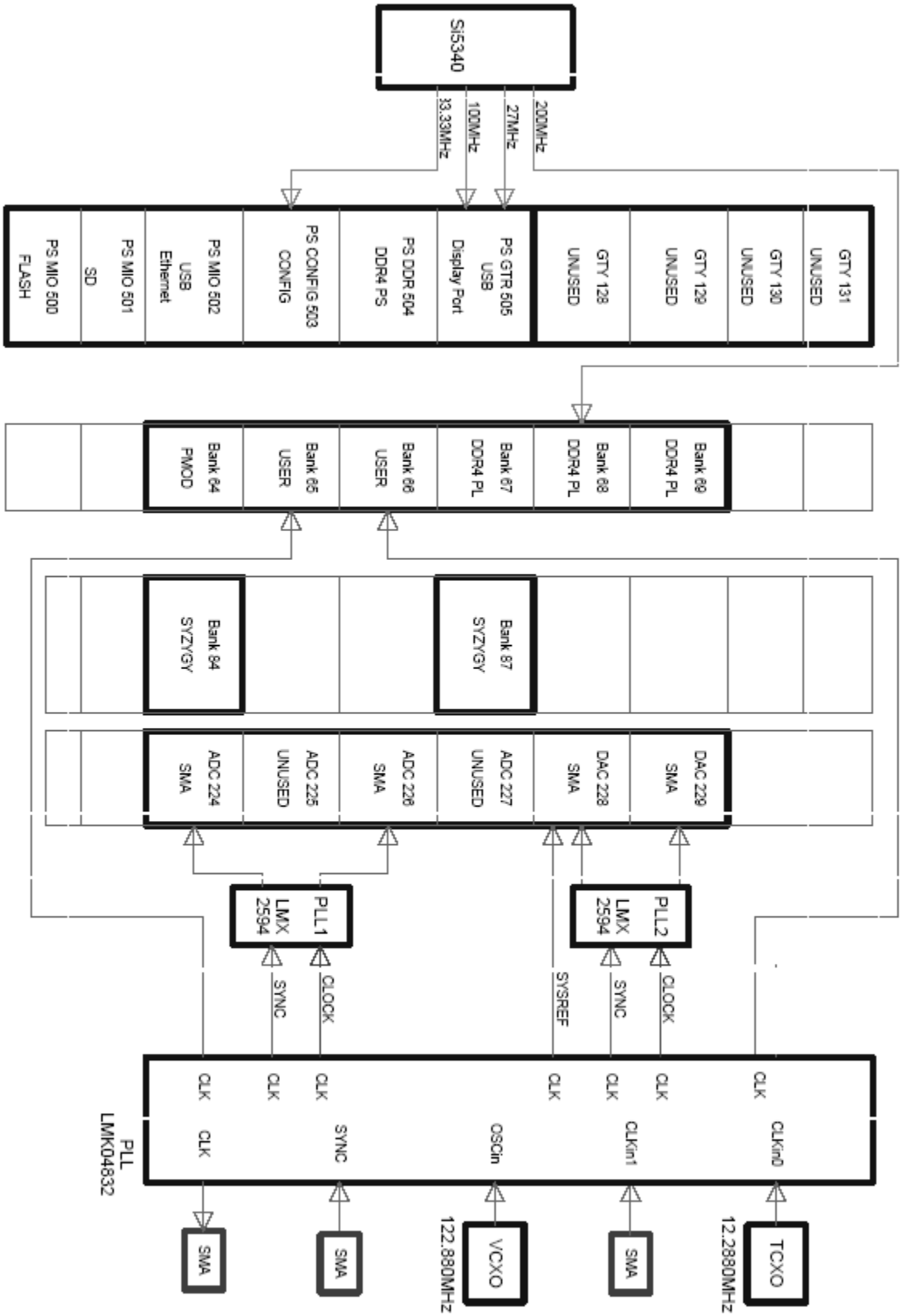

Figure (3): Clock Block Diagram

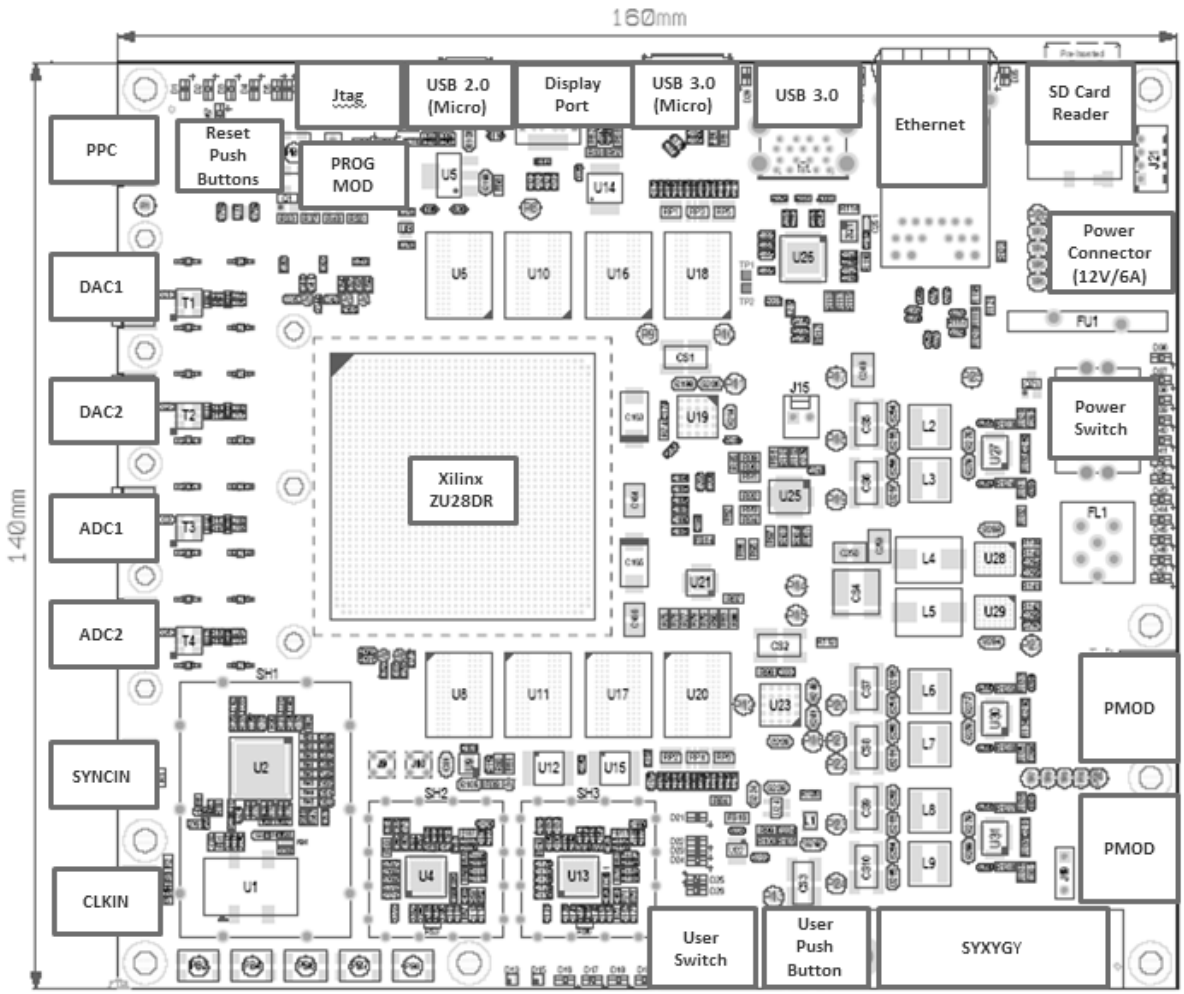

Figure (4): User Interface Ports/Controls

4.0) Main Clocks

The RFSoC_2x2 platform provides combination of fixed, programmable, and adjustable ultra-low-jitter clock sources for different interfaces as summarized by the table (2).

Source	Part Number (Manufacturer)	Default Value	Clock Function
U54	Si5340A	33.3333, 27, 100 and 200 MHz / Programmable	PS, GTR505 & DDR4
U2	LMK04832NKD	Programmable	Clock Jitter Cleaner (ADC/DAC)
U4	LMX2594RHA	Programmable	DAC 228 & DAC 229
U13	LMX2594RHA	Programmable	ADC 224 & ADC 226
U72	ECS-TXO-5032-122.8	12.288 MHz	Clock Jitter Cleaner Reference (ADC/DAC)
U1	ABLNO-V-122.88MHZ	122.88 MHz	Clock Jitter Cleaner Reference (ADC/DAC)
ZQ1	FA-238 25.0000MB	25 MHz	USB3 HUB Controller
ZQ2	FA-238 25.0000MB	25 MHz	Ethernet
ZQ3	FA-238 24.0000MB	24 MHz	USB2 ULPI Transceiver (U48)
ZQ4	7M48072002	48 MHz	U54 Clock Generator Reference
ZQ5	FA-238 24.0000MB	24 MHz	USB2 ULPI Transceiver (U55)
ZQ6	9HT10-32.768KDZF-T	32.768 KHz	PS_PADI/PS_PADO RTC
ZQ7	FA-238V 12.0000MB-W3	12.00 MHz	FTDI / USB Reference CLK
J7	SMA Connector	Variable	CLK-IN for U2 Clock Cleaner (ADC/DAC)
J6	SMA Connector	Variable	SYNC-IN for U2 Clock Cleaner (ADC/DAC)

Table (2): Main Clocks

►*The any-frequency, any-output Si5340 (U54) clock generator combines a wide-band PLL with proprietary MultiSynth fractional synthesizer technology to offer a versatile and high performance clock generator platform. This highly flexible architecture is capable of synthesizing a wide range of integer and no-integer related frequencies up to 712.5 MHz on 4 differential clock outputs while delivering sub-100 fs rms phase jitter performance with 0 ppm error. Each of the clock outputs can be assigned its own format and output voltage enabling the Si5340 to replace multiple clock ICs and oscillators with a single device making it a true "clock tree on a chip".*

The Si5340 can be quickly and easily reconfigured using the **ClockBuilder Pro** software. The device can be programmed in circuit via I2C and SPI serial interfaces or using Silicon Labs' **CBPROG** dongle and the J19 header. **The NVM of the Si5340 can be programmed only once on the RFSoC_2x2 platform.**

https://www.silabs.com/products/development-tools/software/clockbuilder-pro-software

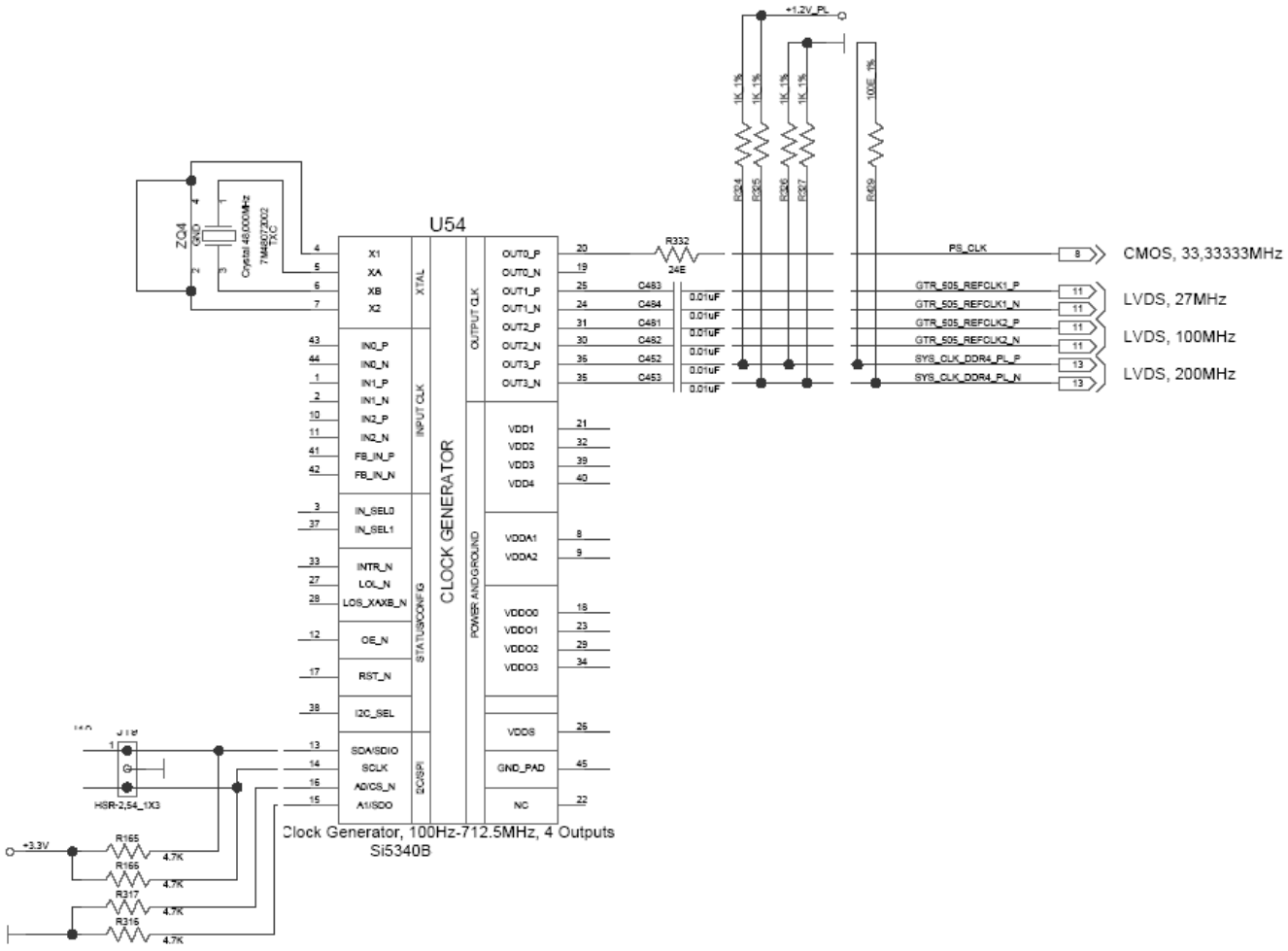

Figure (5): Si5340 Clock Generator Block Diagram

Table (3) provides summary of clock outputs of the Si5340 (U54) clock generator.

Output #	Signal Name	CLK Value	Destination	FPGA Pin #
OUT0_P	PS_CLK	33.33333 MHz	Processor CLK	AC30
OUT0_N	-			-
OUT1_P	GTR_505_REFCLK1_P	27 MHz	USB0, USB1 & Display Port	AJ34
OUT1_N	GTR_505_REFCLK1_N			AJ35
OUT2_P	GTR_505_REFCLK2_P	100 MHz	USB0, USB1 & Display Port	AG34
OUT2_N	GTR_505_REFCLK2_N			AG35
OUT3_P	SYS_CLK_DDR4_PL_P	200 MHz	DDR4 CLK (PL)	G13
OUT3_N	SYS_CLK_DDR4_PL_N			G12

Table (3): Summary of the Si5340 (U54) Clock Outputs

►*The LMX2594 (U4 & U13) is a high performance wideband synthesizer (PLL with integrated VCO). The output frequency range is from 20 MHz to 5.5 GHz. The VCO core covers an octave from 3.55 to 7.1 GHz. The output channel divider covers the frequency range from 20 MHz to the low bound of the VCO core.*

The input signal frequency has a wide range from 5 to 1400 MHz. Following the input, there is an programmable OSCin doubler, a pre-R divider (previous to multiplier), a multiplier, and then a post-R divider (after multiplier) for flexible frequency planning between the input (OSCin) and the phase detector.

The phase detector (PFD) can take frequencies from 5 to 200 MHz, but also has extended modes down to 0.25 MHz and up to 400 MHz. The phase-lock loop (PLL) contains a Sigma-Delta modulator (1st to 4th order) for fractional N-divider values. The fractional denominator is programmable to 32-bit long, allowing a very fine resolution of frequency step. There is a phase adjust feature that allows shifting of the output phase in relation to the input (OSCin) by a fraction of the size of the fractional denominator.

The output power is programmable and can be designed for high power at a specific frequency by the pullup component at the output pin.

The digital logic is a standard 4-wire SPI or uWire interface and is 1.8-V and 3.3-V compatible.

The onboard LMX2594 should be programmed using Texas Instruments' TICS PRO software (http://www.ti.com/tool/TICSPRO-SW)

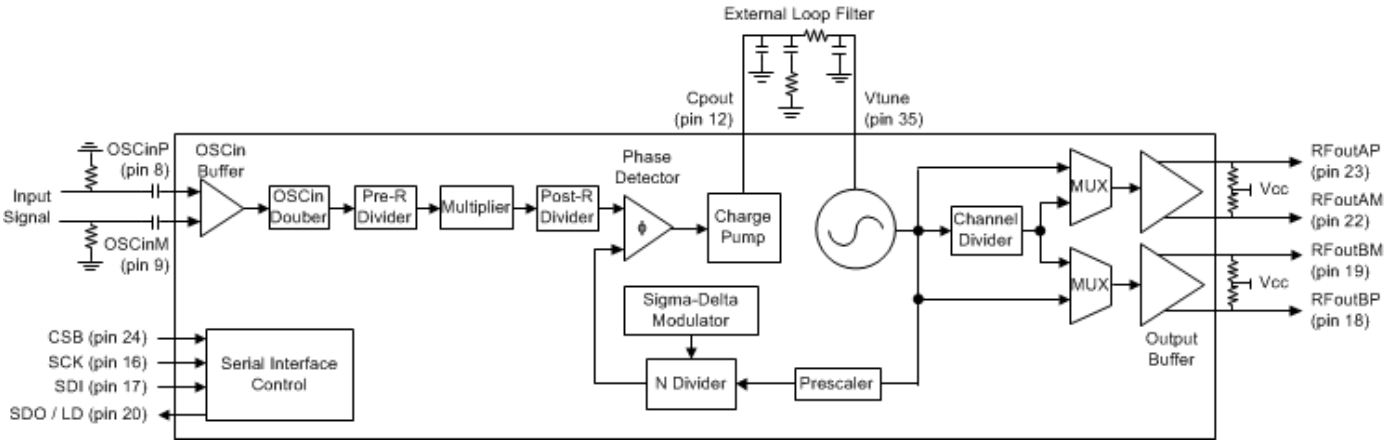

Figure (6): LMX2594 Block Diagram

5.0) DDR4 Memory

The RFSoC_2x2 platform provides access to 4GB of DDR4 memory for the PS and PL side each. (Part Number: MT40A512M16LY-075:E).

Table (4) and (5) illustrate the FPGA bank assignment for the DDR4 PL and PS sides.

DDR4 Signal Name (PL Side)	FPGA Pin #
DDR4_PL_A0	H6
DDR4_PL_A1	G7
DDR4_PL_A10	H11

DDR4_PL_A11	A11
DDR4_PL_A12	E12
DDR4_PL_A13	B14
DDR4_PL_A14	K13
DDR4_PL_A15	D14
DDR4_PL_A16	E13
DDR4_PL_A2	B13
DDR4_PL_A3	F10
DDR4_PL_A4	F11
DDR4_PL_A5	D13
DDR4_PL_A6	J7
DDR4_PL_A7	A15
DDR4_PL_A8	A12
DDR4_PL_A9	A14
DDR4_PL_ACT_N	H13
DDR4_PL_ALERT_N	G8
DDR4_PL_BA0	E14
DDR4_PL_BA1	H10
DDR4_PL_BG0	H12
DDR4_PL_CK_C	J10
DDR4_PL_CK_T	J11
DDR4_PL_CKE	F12
DDR4_PL_CS_N	E11
DDR4_PL_DM_DBI_N0	J15
DDR4_PL_DM_DBI_N1	N14
DDR4_PL_DM_DBI_N2	D18
DDR4_PL_DM_DBI_N3	G17
DDR4_PL_DM_DBI_N4	F21
DDR4_PL_DM_DBI_N5	J23
DDR4_PL_DM_DBI_N6	C23
DDR4_PL_DM_DBI_N7	N20
DDR4_PL_DQ0	H17
DDR4_PL_DQ1	J16
DDR4_PL_DQ10	M15
DDR4_PL_DQ11	M12
DDR4_PL_DQ12	M17
DDR4_PL_DQ13	L12
DDR4_PL_DQ14	N15
DDR4_PL_DQ15	N13
DDR4_PL_DQ16	A19
DDR4_PL_DQ17	A16

DDR4_PL_DQ18	C17
DDR4_PL_DQ19	C16
DDR4_PL_DQ2	H16
DDR4_PL_DQ20	B19
DDR4_PL_DQ21	D16
DDR4_PL_DQ22	A17
DDR4_PL_DQ23	D15
DDR4_PL_DQ24	E18
DDR4_PL_DQ25	F16
DDR4_PL_DQ26	E17
DDR4_PL_DQ27	G15
DDR4_PL_DQ28	G18
DDR4_PL_DQ29	F15
DDR4_PL_DQ3	K16
DDR4_PL_DQ30	E16
DDR4_PL_DQ31	H18
DDR4_PL_DQ32	E24
DDR4_PL_DQ33	D21
DDR4_PL_DQ34	E22
DDR4_PL_DQ35	E21
DDR4_PL_DQ36	F24
DDR4_PL_DQ37	F20
DDR4_PL_DQ38	E23
DDR4_PL_DQ39	G20
DDR4_PL_DQ4	J18
DDR4_PL_DQ40	K24
DDR4_PL_DQ41	G22
DDR4_PL_DQ42	J21
DDR4_PL_DQ43	G23
DDR4_PL_DQ44	L24
DDR4_PL_DQ45	H22
DDR4_PL_DQ46	H23
DDR4_PL_DQ47	H21
DDR4_PL_DQ48	C21
DDR4_PL_DQ49	A24
DDR4_PL_DQ5	K17
DDR4_PL_DQ50	C22
DDR4_PL_DQ51	B24
DDR4_PL_DQ52	B20
DDR4_PL_DQ53	A21
DDR4_PL_DQ54	C20

DDR4_PL_DQ55	A20
DDR4_PL_DQ56	M20
DDR4_PL_DQ57	L20
DDR4_PL_DQ58	L22
DDR4_PL_DQ59	L21
DDR4_PL_DQ6	J19
DDR4_PL_DQ60	N19
DDR4_PL_DQ61	M19
DDR4_PL_DQ62	L23
DDR4_PL_DQ63	L19
DDR4_PL_DQ7	L17
DDR4_PL_DQ8	N17
DDR4_PL_DQ9	M13
DDR4_PL_DQS_C0	K18
DDR4_PL_DQS_C1	L14
DDR4_PL_DQS_C2	B17
DDR4_PL_DQS_C3	F19
DDR4_PL_DQS_C4	D24
DDR4_PL_DQS_C5	H20
DDR4_PL_DQS_C6	A22
DDR4_PL_DQS_C7	K22
DDR4_PL_DQS_T0	K19
DDR4_PL_DQS_T1	L15
DDR4_PL_DQS_T2	B18
DDR4_PL_DQS_T3	G19
DDR4_PL_DQS_T4	D23
DDR4_PL_DQS_T5	J20
DDR4_PL_DQS_T6	B22
DDR4_PL_DQS_T7	K21
DDR4_PL_ODT	F14
DDR4_PL_PAR	B12
DDR4_PL_RST_N	G6
DDR4_PL_TEN	C15
SYS_CLK_DDR4_PL_N	G12
SYS_CLK_DDR4_PL_P	G13

Table (4): DDR4 FPGA Pin Assignment (PL Side)

DDR4 Signal Name (Processor Side)	FPGA Pin #
DDR4_PS_A0	AV31
DDR4_PS_A1	AW28
DDR4_PS_A10	AT31
DDR4_PS_A11	AT32
DDR4_PS_A12	AT30
DDR4_PS_A13	AU32
DDR4_PS_A14	AR28
DDR4_PS_A15	AP30
DDR4_PS_A16	AP28
DDR4_PS_A2	AV28
DDR4_PS_A3	AU29
DDR4_PS_A4	AW31
DDR4_PS_A5	AU28
DDR4_PS_A6	AL29
DDR4_PS_A7	AM30
DDR4_PS_A8	AM29
DDR4_PS_A9	AP29
DDR4_PS_ACT_N	AL30
DDR4_PS_ALERT_N	AL32
DDR4_PS_BA0	AN30
DDR4_PS_BA1	AM32
DDR4_PS_BG0	AN32
DDR4_PS_CK_C	AV30
DDR4_PS_CK_T	AU30
DDR4_PS_CKE	AW30
DDR4_PS_CS_N	AW29
DDR4_PS_DM_DBI_N0	AU23
DDR4_PS_DM_DBI_N1	AT27
DDR4_PS_DM_DBI_N2	AL24
DDR4_PS_DM_DBI_N3	AM27
DDR4_PS_DM_DBI_N4	AV36
DDR4_PS_DM_DBI_N5	AT35
DDR4_PS_DM_DBI_N6	AM36
DDR4_PS_DM_DBI_N7	AJ32
DDR4_PS_DQ0	AW25
DDR4_PS_DQ1	AW24
DDR4_PS_DQ10	AU25
DDR4_PS_DQ11	AR27
DDR4_PS_DQ12	AU27
DDR4_PS_DQ13	AV26

DDR4_PS_DQ14	AV27
DDR4_PS_DQ15	AW26
DDR4_PS_DQ16	AP25
DDR4_PS_DQ17	AP24
DDR4_PS_DQ18	AP23
DDR4_PS_DQ19	AN25
DDR4_PS_DQ2	AV25
DDR4_PS_DQ20	AM25
DDR4_PS_DQ21	AK24
DDR4_PS_DQ22	AN23
DDR4_PS_DQ23	AK23
DDR4_PS_DQ24	AK26
DDR4_PS_DQ25	AL25
DDR4_PS_DQ26	AK28
DDR4_PS_DQ27	AK27
DDR4_PS_DQ28	AN27
DDR4_PS_DQ29	AN26
DDR4_PS_DQ3	AW23
DDR4_PS_DQ30	AN28
DDR4_PS_DQ31	AM28
DDR4_PS_DQ32	AU39
DDR4_PS_DQ33	AU38
DDR4_PS_DQ34	AU37
DDR4_PS_DQ35	AU35
DDR4_PS_DQ36	AV38
DDR4_PS_DQ37	AW36
DDR4_PS_DQ38	AV35
DDR4_PS_DQ39	AW35
DDR4_PS_DQ4	AV23
DDR4_PS_DQ40	AU33
DDR4_PS_DQ41	AV33
DDR4_PS_DQ42	AW34
DDR4_PS_DQ43	AW33
DDR4_PS_DQ44	AR34
DDR4_PS_DQ45	AR33
DDR4_PS_DQ46	AP33
DDR4_PS_DQ47	AP34
DDR4_PS_DQ48	AL39
DDR4_PS_DQ49	AM38
DDR4_PS_DQ5	AV22
DDR4_PS_DQ50	AM39

DDR4_PS_DQ51	AN38
DDR4_PS_DQ52	AM35
DDR4_PS_DQ53	AM34
DDR4_PS_DQ54	AN36
DDR4_PS_DQ55	AN35
DDR4_PS_DQ56	AK32
DDR4_PS_DQ57	AK31
DDR4_PS_DQ58	AJ31
DDR4_PS_DQ59	AJ30
DDR4_PS_DQ6	AR24
DDR4_PS_DQ60	AH30
DDR4_PS_DQ61	AG32
DDR4_PS_DQ62	AF32
DDR4_PS_DQ63	AG30
DDR4_PS_DQ7	AR23
DDR4_PS_DQ8	AT25
DDR4_PS_DQ9	AP26
DDR4_PS_DQS_C0	AU24
DDR4_PS_DQS_C1	AT26
DDR4_PS_DQS_C2	AM24
DDR4_PS_DQS_C3	AL27
DDR4_PS_DQS_C4	AW37
DDR4_PS_DQS_C5	AU34
DDR4_PS_DQS_C6	AN37
DDR4_PS_DQS_C7	AH32
DDR4_PS_DQS_T0	AT24
DDR4_PS_DQS_T1	AR26
DDR4_PS_DQS_T2	AM23
DDR4_PS_DQS_T3	AL26
DDR4_PS_DQS_T4	AV37
DDR4_PS_DQS_T5	AT34
DDR4_PS_DQS_T6	AM37
DDR4_PS_DQS_T7	AH31
DDR4_PS_ODT	AV32
DDR4_PS_PAR	AN31
DDR4_PS_RST_N	AM33

Table (5) DDR4 FPGA Pin Assignment (Processor Side)

6.0) ADC and DAC Ports

The RFSoC_2x2 platform provides access to two ADC and two DAC ports through four SMA connectors. As showed by figures (7) and (8), the ADC and DAC ports are supported through high-performance front panel Mini Circuits **TCM1-83X+** micro Rf transformer with bandwidth ranging from 10 to 8000 MHz. A Pi Attenuator circuit is placed between these Rf transformers and the RF_MPSoC.

Table (6) illustrates FPGA pin assignments for the ADC interfaces.

ADC Signal Name	FPGA Pin #	Connector #
ADC_224_REFCLK_N	AF4	-
ADC_224_REFCLK_P	AF5	-
ADC_226_REFCLK_N	AB4	-
ADC_226_REFCLK_P	AB5	-
ADC_IN01_224_N	AP1	J5
ADC_IN01_224_P	AP2	J5
ADC_IN01_226_N	AF1	J4
ADC_IN01_226_P	AF2	J4

Table (6): ADC Interface Pin Assignment

Table (7) illustrates FPGA pin assignments for the DAC interfaces.

DAC Signal Name	FPGA Pin #	Connector #
DAC_228_REFCLK_N	R4	-
DAC_228_REFCLK_P	R5	-
DAC_228_SYSREF_N	U4	-
DAC_228_SYSREF_P	U5	-
DAC_229_REFCLK_N	N4	-
DAC_229_REFCLK_P	N5	-
DAC_VOUT0_228_N	U1	J3
DAC_VOUT0_228_P	U2	J3
DAC_VOUT0_229_N	J1	J2
DAC_VOUT0_229_P	J2	J2

Table (7): DAC Interface Pin Assignment

Figures (7) and (8) illustrate ADC/DAC interface paths from SMA connectors to the FPGA's ADC/DAC tiles.

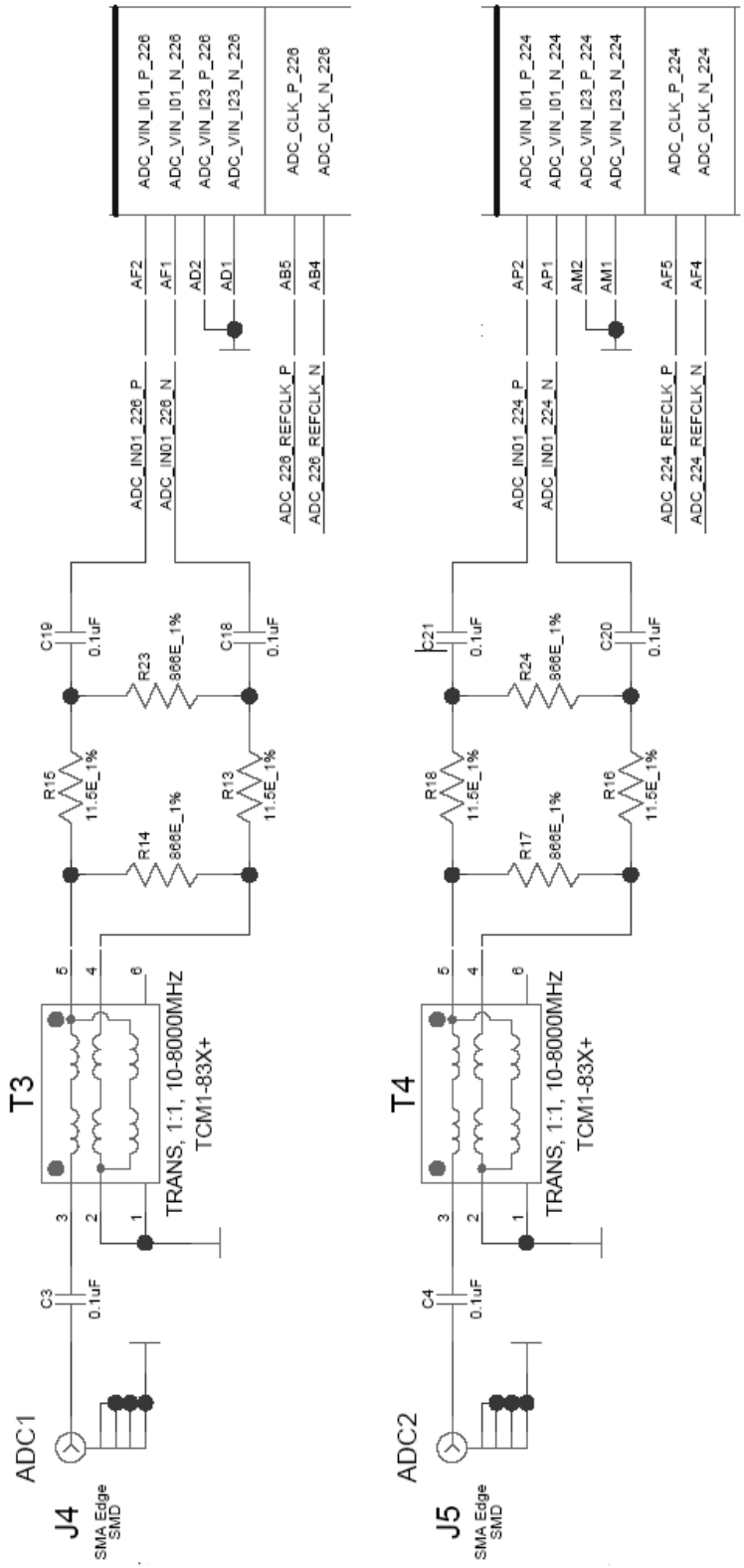

Figure (7): ADC Ports – FPGA Interface

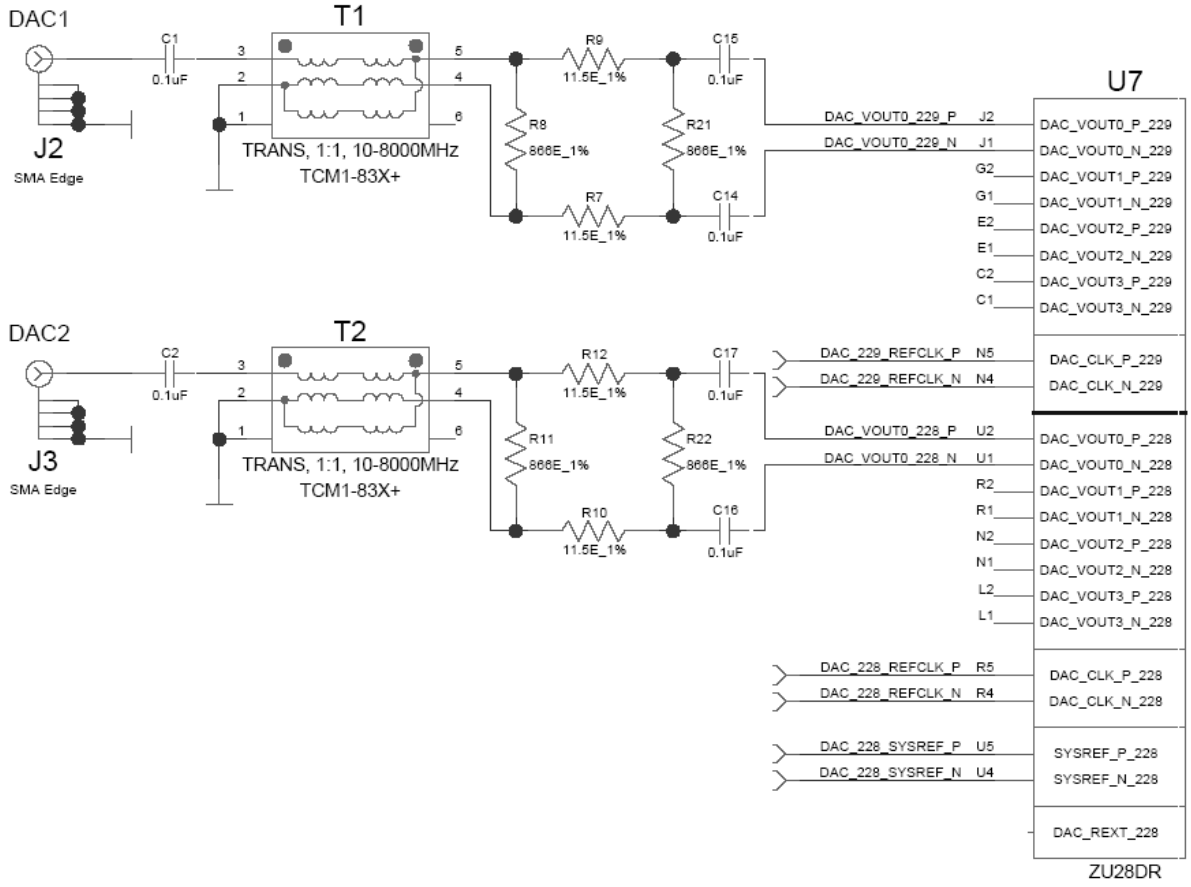

Figure (8): DAC Ports – FPGA Interface

6.1) ADC/DAC Clocks

The Texas Instruments components used for the ADC and DAC ports should be programmed using Texas Instruments' TICS PRO software (http://www.ti.com/tool/TICSPRO-SW) . All LMX2594 components are blank and must be programmed according to the end application.

Figure (9) illustrates high level block configuration of the ADC/DAC channels.

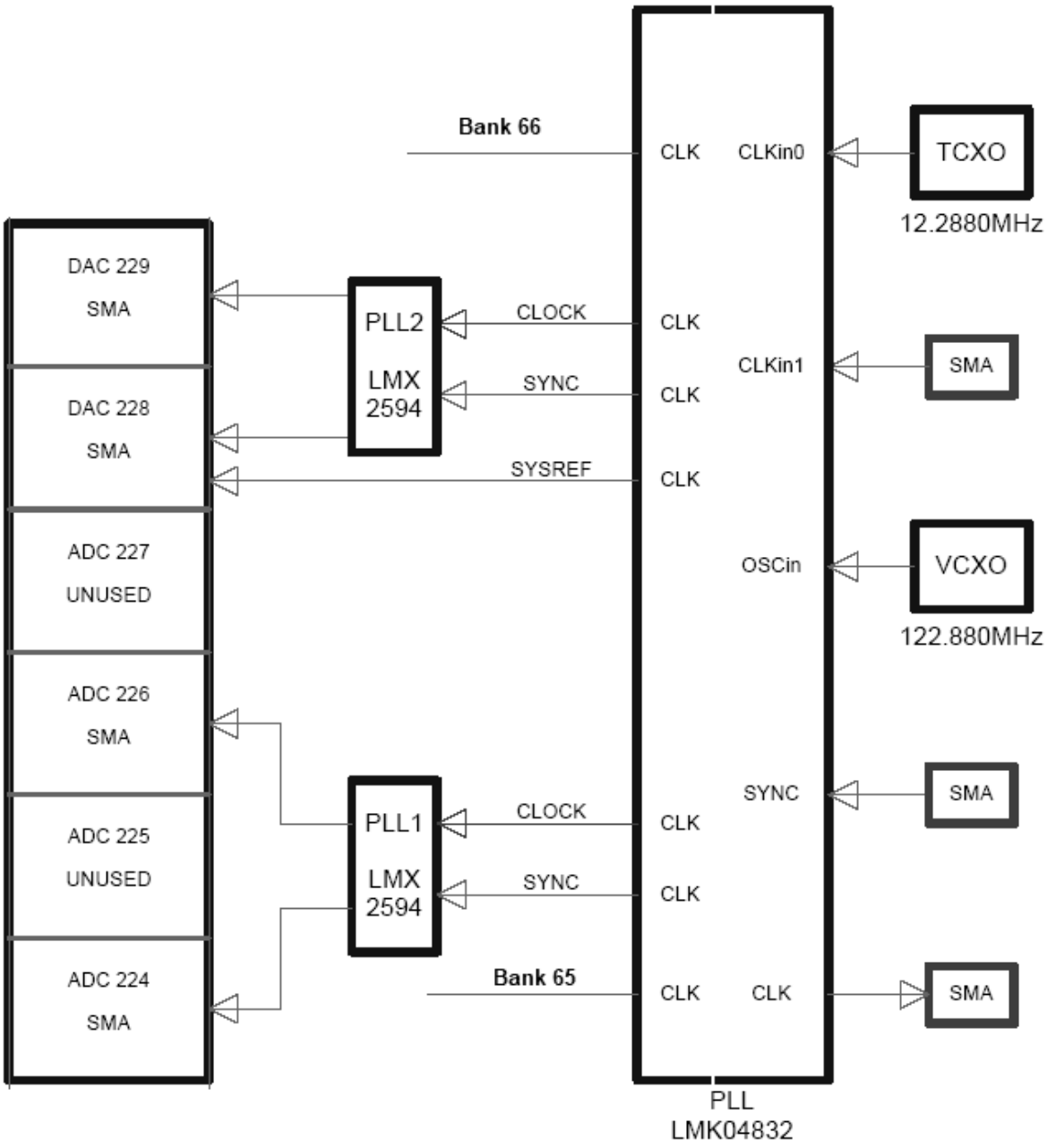

Figure (9): ADC/DAC Clock Configuration

7.0) USB Ports

The RFSoC_2x2 platform provides access to the following USB ports:

- Two USB 3.0 Host ports (J14/stacked) accessing GTR transceiver of the FPGA through a USB Hub controller.
- One USB 3.0 Slave port (J13) connected to one GTR transceiver of the FPGA and the processor's I/Os through two USB 2.0 ULPI transceivers.
- One USB 2.0 Slave port (J11) for UART and JTAG programming of the FPGA.

Reference clock for the USB3.0 serial transceivers is provided by the onboard SI5340 clock generator.

The USB interfaces are protected by ultra-low capacitance TVS Arrays to protect the circuitry against voltage spikes originated from electro static discharge (ESD) and inductive load switching.

Table (8) illustrates FPGA pin assignment for the USB interfaces.

USB Signal Name	FPGA Pin Number	USB Function
MIO52_USB0_CLK	N26	USB 3.0 Slave
MIO53_USB0_DIR	L25	USB 3.0 Slave
MIO54_USB0_D2	M26	USB 3.0 Slave
MIO55_USB0_NXT	J25	USB 3.0 Slave
MIO56_USB0_D0	L26	USB 3.0 Slave
MIO57_USB0_D1	H25	USB 3.0 Slave
MIO58_USB0_STP	H26	USB 3.0 Slave
MIO59_USB0_D3	H27	USB 3.0 Slave
MIO6_PS_USER_PB	W26	USB 3.0 Slave
MIO60_USB0_D4	J26	USB 3.0 Slave
MIO61_USB0_D5	G28	USB 3.0 Slave
MIO62_USB0_D6	K26	USB 3.0 Slave
MIO63_USB0_D7	G29	USB 3.0 Slave
MIO64_USB1_CLK	K27	USB 3.0 Host
MIO65_USB1_DIR	L27	USB 3.0 Host
MIO66_USB1_D2	N27	USB 3.0 Host
MIO67_USB1_NXT	J28	USB 3.0 Host
MIO68_USB1_D0	H29	USB 3.0 Host
MIO69_USB1_D1	M27	USB 3.0 Host
MIO7_USB_RESET_B	T26	
MIO70_USB1_STP	K28	USB 3.0 Host
MIO71_USB1_D3	H28	USB 3.0 Host
MIO72_USB1_D4	J29	USB 3.0 Host
MIO73_USB1_D5	K29	USB 3.0 Host
MIO74_USB1_D6	M28	USB 3.0 Host
MIO75_USB1_D7	N28	USB 3.0 Host
USB0_US_RXN	AE39	USB 3.0 Slave

USB0_US_RXP	AE38	USB 3.0 Slave
USB0_US_TXN	AF37	USB 3.0 Slave
USB0_US_TXP	AF36	USB 3.0 Slave
USB1_DS_RXN	AC39	USB 3.0 Host
USB1_DS_RXP	AC38	USB 3.0 Host
USB1_DS_TXN	AD37	USB 3.0 Host
USB1_DS_TXP	AD36	USB 3.0 Host
MIO18_UART0_RXD	Y27	USB 2.0 Slave (UART/JTAG)
MIO19_UART0_TXD	W28	USB 2.0 Slave (UART/JTAG)

Table (8): USB Interface Pin Assignment

8.0) SDIO Interface

The RFSoC_2x2 platform supports a secure digital input/output (SDIO) interface providing access to general purpose non-volatile SDIO memory cards and peripherals. The SDIO signals are connected to the PS bank 501 of the onboard Zynq UltraScale+ FPGA. A SD 3.0-compliant voltage level-translator (P4856CX25/C) is present between the onboard Zynq UltraScale+ RFSoC FPGA and the SD card connector (J18). The JP1 connector (marked as "Prog Mode on figure 4) has the factory default setting to boot through the SD card interface.

Table (9) illustrates FPGA pin assignment for the SDIO Interface.

FPGA Signal Name	FPGA Pin Number
MIO39_SDIO_SEL	B28
MIO40_SDIO_DIR_CMD	D26
MIO41_SDIO_DIR_DAT0	C28
MIO42_SDIO_DIR_DAT1	E28
MIO44_SDIO_PROTECT	F27
MIO45_SDIO_DETECT	G27
MIO46_SDIO_DAT0	A29
MIO47_SDIO_DAT1	C29
MIO48_SDIO_DAT2	D29
MIO49_SDIO_DAT3	B29
MIO50_SDIO_CMD	F29
MIO51_SDIO_CLK	E29

Table (9): SDIO Port's FPGA Pin Assignment

9.0) 10/100/1000 Mbps Ethernet

The RFSoC_2x2 platform provides access to one 10/100/1000 Mbps Ethernet port (J16) supported by Texas Instruments DP83867IRPAP PHY chip connected to the processor's I/Os of the FPGA.

The DP83867 device is a fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. This device interfaces directly to the MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII), the IEEE 802.3 Gigabit Media Independent Interface (GMII) or Reduced GMII (RGMII). The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

The Ethernet activities are reported by the following LEDs:

- LINK (on the RJ45 connector): By default, this pin indicates that link is established.
- ACT: (on the RJ45 connector): By default, this pin indicates receive or transmit activity.
- D35: (on the board/next to the RJ45 connector): By default, this pin indicates that 1000BASE-T link is established.

Table (10) illustrates FPGA pin assignment for the Ethernet interface.

FPGA Signal Name	FPGA Pin Number
MIO26_ETH_TX_CLK	G25
MIO27_ETH_TX_D0	C25
MIO28_ETH_TX_D1	F25
MIO29_ETH_TX_D2	B25
MIO30_ETH_TX_D3	D25
MIO31_ETH_TX_CTRL	C26
MIO32_ETH_RX_CLK	A26
MIO33_ETH_RX_D0	A27
MIO34_ETH_RX_D1	B27
MIO35_ETH_RX_D2	E26
MIO36_ETH_RX_D3	C27
MIO37_ETH_RX_CTRL	F26

Table (10): Ethernet Port's FPGA Pin Assignment

10.0) Display Port

The RFSoC_2x2 platform provides access to one Display Port (J12) connected to the processor's single-ended and serial I/Os of the FPGA.

Reference clock for the Display Port GTR serial transceivers is provided by the onboard SI5340 clock generator.

Table (11) illustrates FPGA pin assignment for the Display Port interface.

FPGA Signal Name	FPGA Pin Number
DP_TX0_N	AH37
DP_TX0_P	AH36
DP_TX1_N	AK37

DP_TX1_P	AK36
MIO22_DP_AUX_OUT	AG18
MIO23_DP_HPD	AH18
MIO24_DP_OE	AF20
MIO25_DP_AUX_IN	AF19

Table (11): Display Port's FPGA Pin Assignment

11.0) 1-PPS Interface

The RFSoC_2x2 platform provides access to one 1-PPS interface through one SMA connector (J1), one Comparator, one 8-bit ADC (3MSPS), and one Schmitt-Trigger Buffer.

Table (12) illustrates FPGA pin assignment for the 1-PPS interface.

FPGA Signal Name	FPGA Pin Number
IRIG_ADC_CS_N	AG13
IRIG_ADC_SCLK	AG12
IRIG_ADC_SDO	AG14
IRIG_COMP_OUT	AH13
IRIG_TRIG_OUT	AH12

Table (12): 1-PPS Port's FPGA Pin Assignment

12.0) PMOD Ports

The RFSoC_2x2 platform provides access to two 2x6 PMOD ports (J22 and J23) for interfacing to Digilent's dauther cards (https://store.digilentinc.com/pmod-modules-connectors)

Table (13) illustrates FPGA pin assignment for the PMOD interfaces.

FPGA Signal Name	FPGA Pin Number
PMOD0_0_F	AT16
PMOD0_1_F	AW16
PMOD0_2_F	AV16
PMOD0_3_F	AU15
PMOD0_4_F	AV13
PMOD0_5_F	AU13
PMOD0_6_F	AU14
PMOD0_7_F	AT15
PMOD1_0_F	AJ15
PMOD1_1_F	AL15
PMOD1_2_F	AJ16

PMOD1_3_F	AK16
PMOD1_4_F	AM17
PMOD1_5_F	AP15
PMOD1_6_F	AL16
PMOD1_7_F	AK17

Table (13): PMOD Ports' FPGA Pin Assignment

13.0) SYZYGY Port

The RFSoC_2x2 platform platform provides access to one Standard SYZYGY port (J17) with the following features:

- 40-pin 0.8mm Samtec connector
- 5V, 3.3V fixed voltages
- Programmable VIO supply
- MCU for peripheral personality and VIO setting
- 8 differential pairs (or 16 single-ended signals)
- 12 additional single-ended signals
- Dedicated clock inputs/outputs

The power supply is programmable from 1.2V to 3.3V by using the on-board MCU (U22) and configuration codes shown by the table (14).

VOUT	DAC Code	DAC Voltage
3.3V	18	0.058V
2.5V	312	1.005V
1.8V	569	1.833V
1.2V	789	2.542V

Table (14): SYZYGY Voltage Configuration

The power status LED (D46) will only turn on when a module is plugged to the SYZYGY connector.

Table (15) illustrates FPGA pin assignment for the SYZYGY interface.

FPGA Signal Name	FPGA Pin Number
SYZYGY_C2P_CLKN	B9
SYZYGY_C2P_CLKP	B10
SYZYGY_P2C_CLKN	AV5
SYZYGY_P2C_CLKP	AV6
SYZYGY_S0_D0P	AT7
SYZYGY_S1_D1P	F6
SYZYGY_S10_D4N	AW3

SYZYGY_S11_D5N	A6
SYZYGY_S12_D6P	AV3
SYZYGY_S13_D7P	C8
SYZYGY_S14_D6N	AV2
SYZYGY_S15_D7N	C7
SYZYGY_S16	AV7
SYZYGY_S17	B8
SYZYGY_S18	AV8
SYZYGY_S19	C5
SYZYGY_S2_D0N	AT6
SYZYGY_S20	AU8
SYZYGY_S21	A5
SYZYGY_S22	AU7
SYZYGY_S23	D6
SYZYGY_S24	AR7
SYZYGY_S25	B5
SYZYGY_S26	AR6
SYZYGY_S27	C6
SYZYGY_S3_D1N	E6
SYZYGY_S4_D2P	AU2
SYZYGY_S5_D3P	E9
SYZYGY_S6_D2N	AU1
SYZYGY_S7_D3N	E8
SYZYGY_S8_D4P	AW4
SYZYGY_S9_D5P	A7
SYZYGY_VIO_EN	AR13

Table (15): SYZYGY Port's FPGA Pin Assignment

14.0) LEDs , User Switch & Pushbuttons

The RFSoC_2x2 platform provides user LEDs, XDAC headers, user I/O headers, and Push Buttons.

Table (16) illustrates FPGA pin assignment and reference designators for each interface.

FPGA Signal Name	FPGA Pin Number	Reference Designator
PL_LEDRGB0_B	AW11	D13
PL_LEDRGB0_G	AT11	D13
PL_LEDRGB0_R	AV11	D13
PL_LEDRGB1_B	AR11	D15
PL_LEDRGB1_G	AN12	D15
PL_LEDRGB1_R	AN13	D15

PL_URST	AP9	PB8
PL_USER_LED0_W	AR12	D16
PL_USER_LED1_W	AT12	D17
PL_USER_LED2_W	AV12	D18
PL_USER_LED3_W	AU12	D19
PL_USER_PB0	AM7	PB2
PL_USER_PB1	AM8	PB4
PL_USER_PB2	AN8	PB6
PL_USER_PB3	AP8	PB7
MIO6_PS_PB	W26	PB9
PS_PORN_N	AB29	PB1
PS_SRST_N	AB28	PB5
PS_PROG_N	AA27	PB3
PL_USER_SW1	AT10	S1: KEY 1
PL_USER_SW2	AU10	S1: KEY 2
PL_USER_SW3	AV10	S1: KEY 3
PL_USER_SW4	AW10	S1: KEY 4
MIO4_PS_LED0_G	V26	D30
MIO5_PS_LED1_G	AA26	D32

Table (16): User Interface FPGA Pin Assignment

15.0) Configuration

The RFSoC_2x2 platform can be configured through its Jtag (J8), USB 2 (J11) or MicroSD (J18) ports. The mode select is controlled through inserting shunt on the JP1 header next to the Jtag connector (J8) with connection on pins 1-2 for the SD and 2-3 for the Jtag mode. SD cards class 10 are recommended.