Runtime-First FPGA Interchange Routing Contest @ ISFPGA'24

Eddie Hung, Chris Lavin, Zak Nafziger, Alireza Kaviani

4 March 2024

AMD
together we advance_

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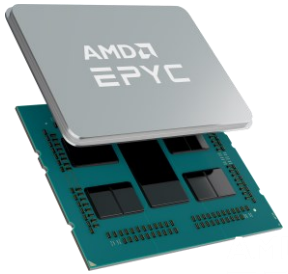


128 x CPU cores
512GB RAM

4 x Instinct™ MI210 GPUs

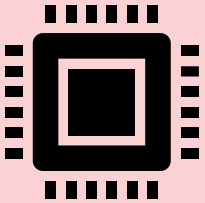
Goals

1. Demonstrate utility and efficiency of the FPGA Interchange Format
2. Encourage innovation into FPGA backend (place-and-route) problems

FPGA Interchange Format: “IR” for Backend Implementation

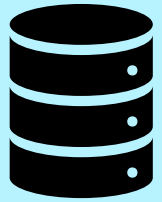
- Everything you need to build your own router for real devices
  - (And placer, too!)
- Allows the efficient exchange of design data, even at industrial scales

DEVICE RESOURCES



What the FPGA looks like

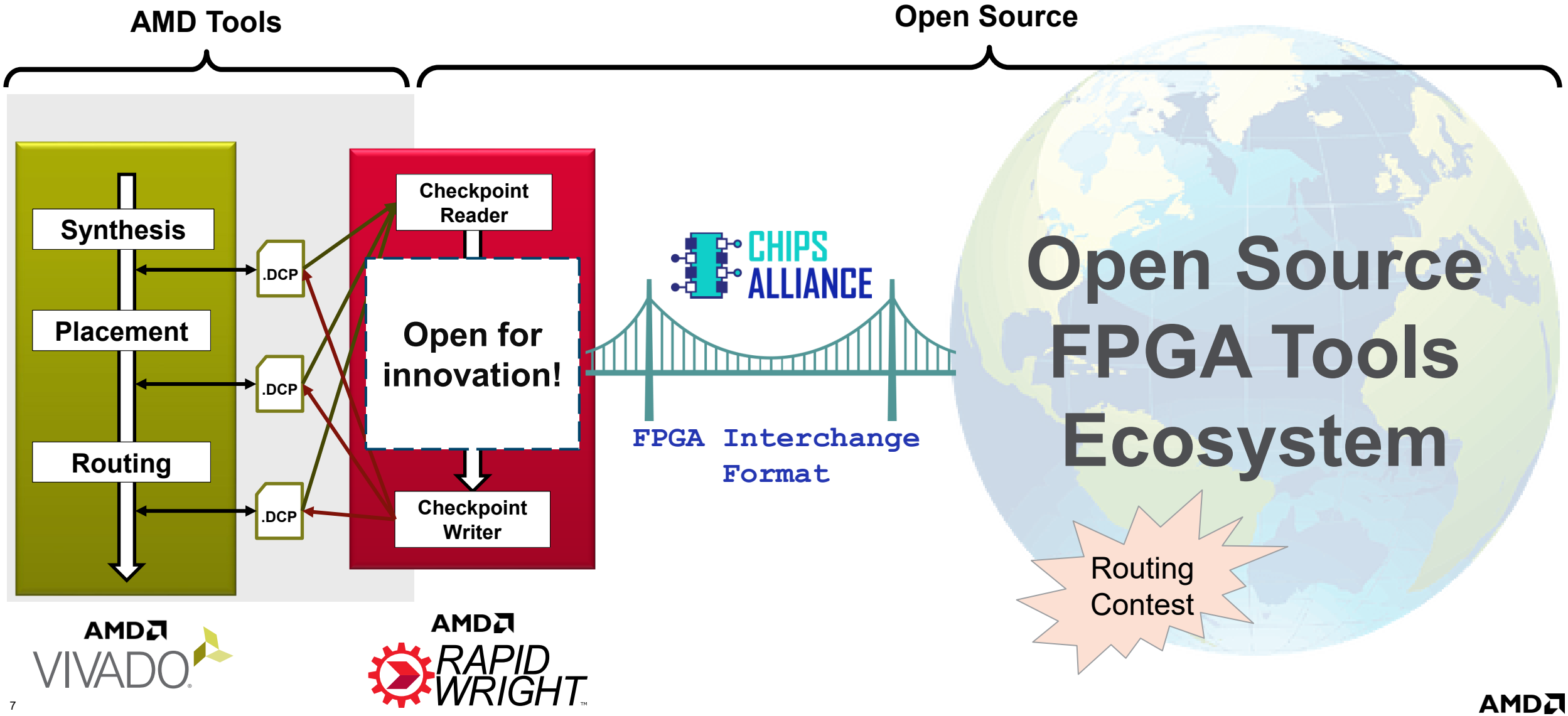
DESIGN NETLISTS



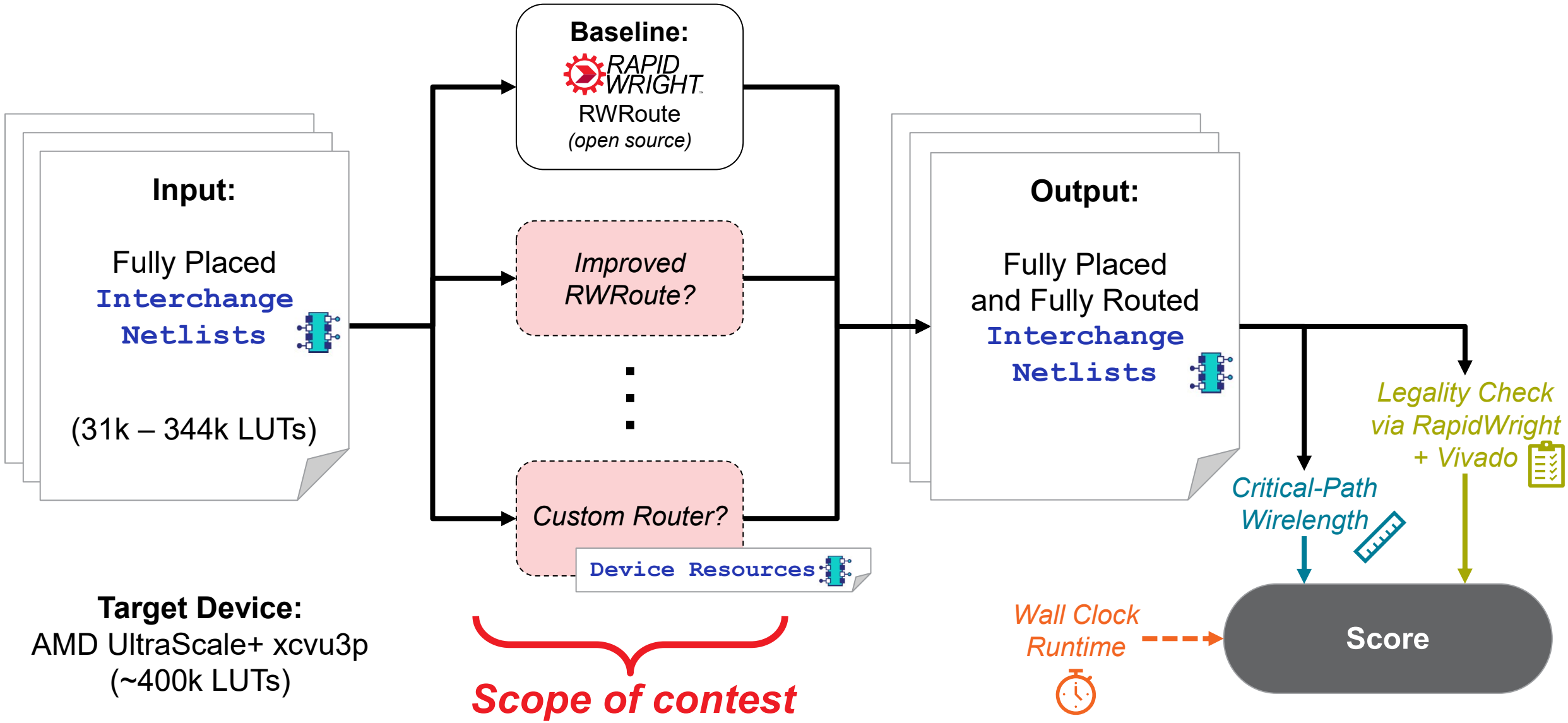
What and where of placement and routing

A vendor neutral, open source format

FPGA Interchange: Building a Bridge to the FPGA Backend



Contest Framework



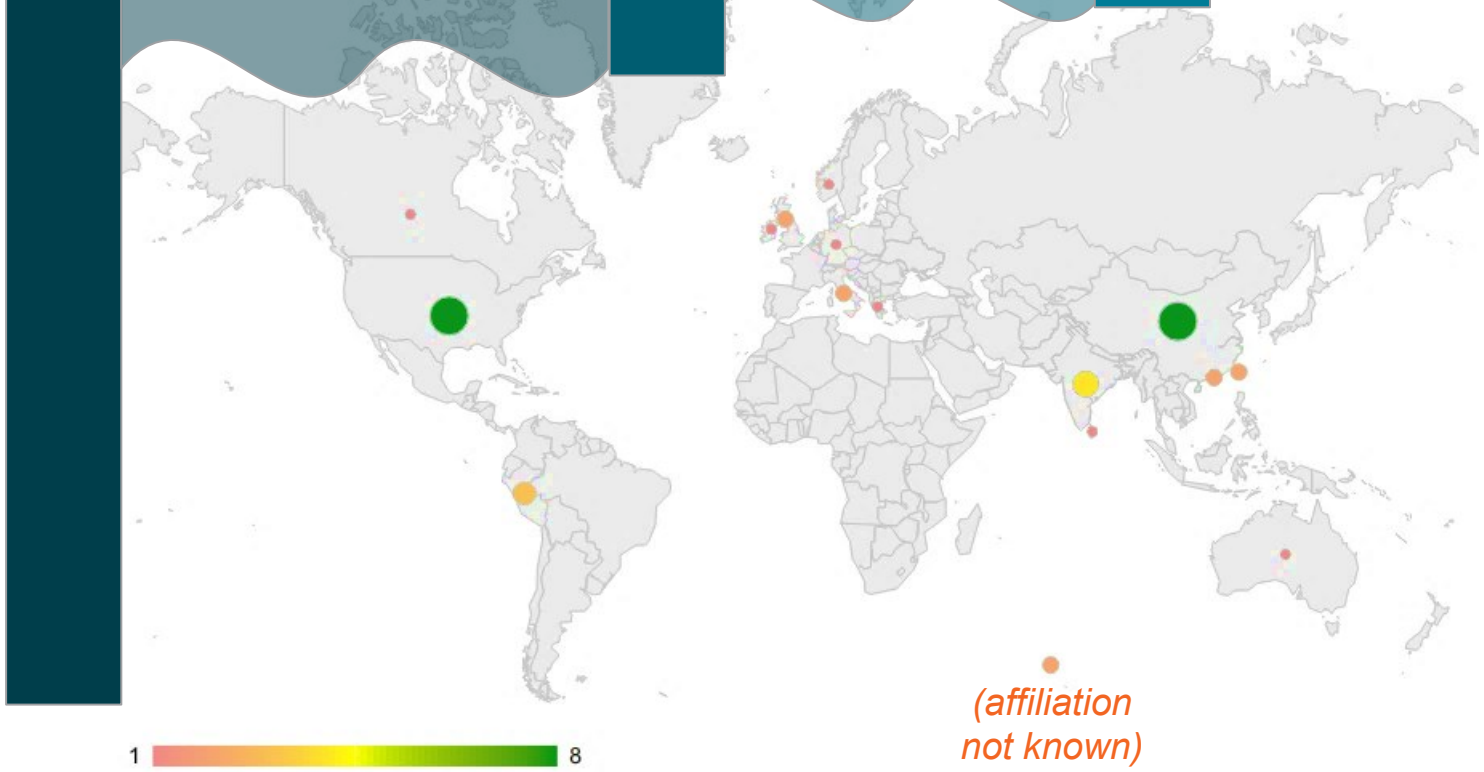
Contest Statistics

40
Teams
Registered
(>150 participants)

13
Alpha
Submissions

10
Final Submissions

5



(affiliation not known)

1st $2,500 USD

2nd $1,500

3rd $1,000

4th $500

5th $500

50% contingent on open source release

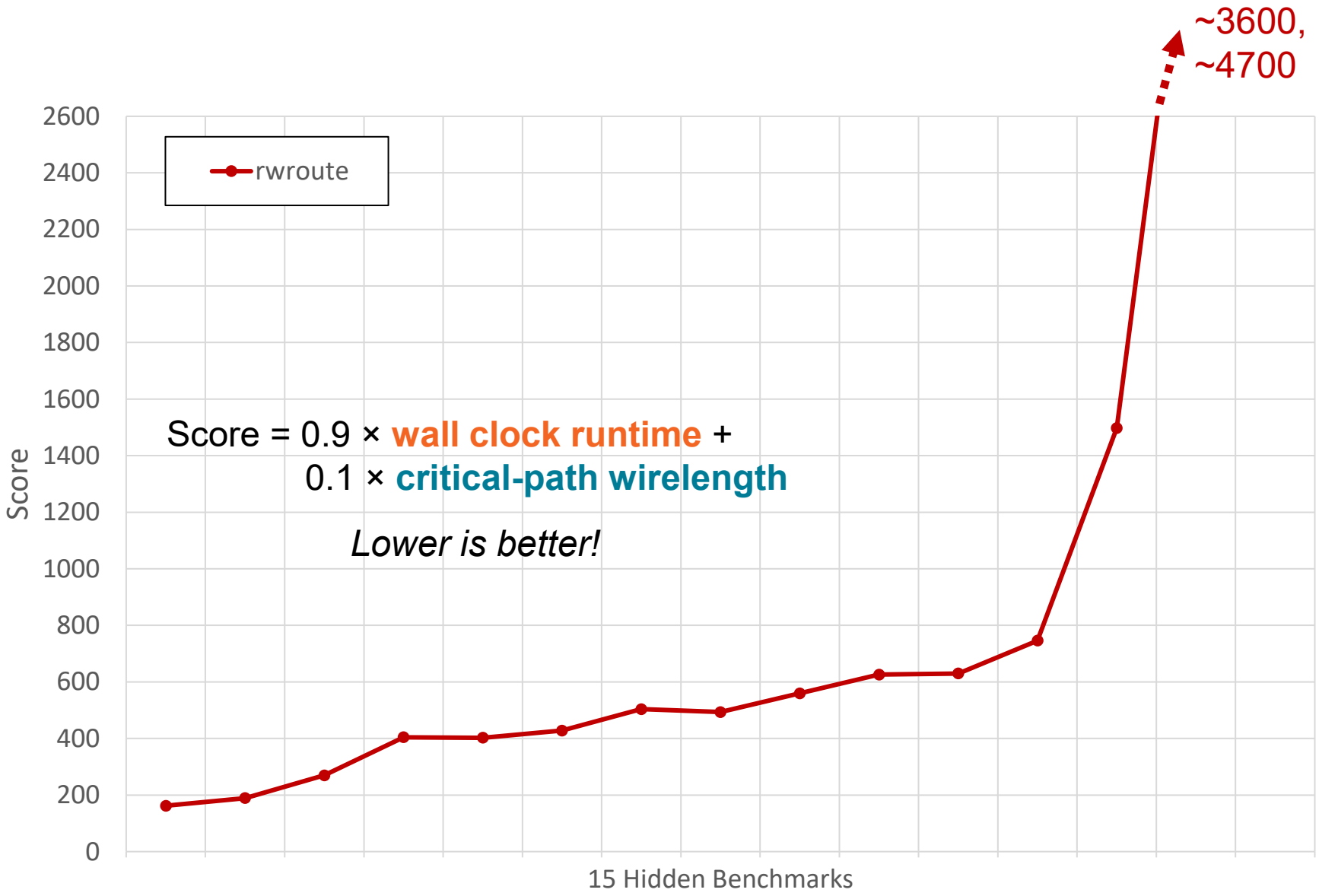
Top 5 Teams (Alphabetical Order)

- **AceRoute** *(Peking University/DeePoly Technology)*
  - Ziyun Zhang, Xinming Wei, Sunan Zou, Jiaxi Zhang, Ping Fan; *Advisor:* Guojie Luo
- **Team Cuckoo** *(Peking University)*
  - Jiarui Wang, Xun Jiang, Chunyuan Zhao; *Advisor:* Yibo Lin
- **CUFR** *(The Chinese University of Hong Kong)*
  - Xinshi Zang, Wenhao Lin, Shiju Lin, Qin Luo; *Advisor:* Evangeline F.Y. Young
- **GRoute** *(University of Guelph)*
  - Dani Maarouf, Timothy Martin, Charlotte Barnes; *Advisors:* Shawki Areibi, Gary Grewal
- **Hao^3** *(University of Science and Technology of China)*
  - Wenbin Teng, Qianyu Cheng, Zhendong Zheng, Binze Jiang, Yixuan Zhu, Zihan Wang
    Advisors: Teng Wang, Chao Wang

Runtime-First FPGA Interchange Routing Contest @ ISFPGA'24

Results

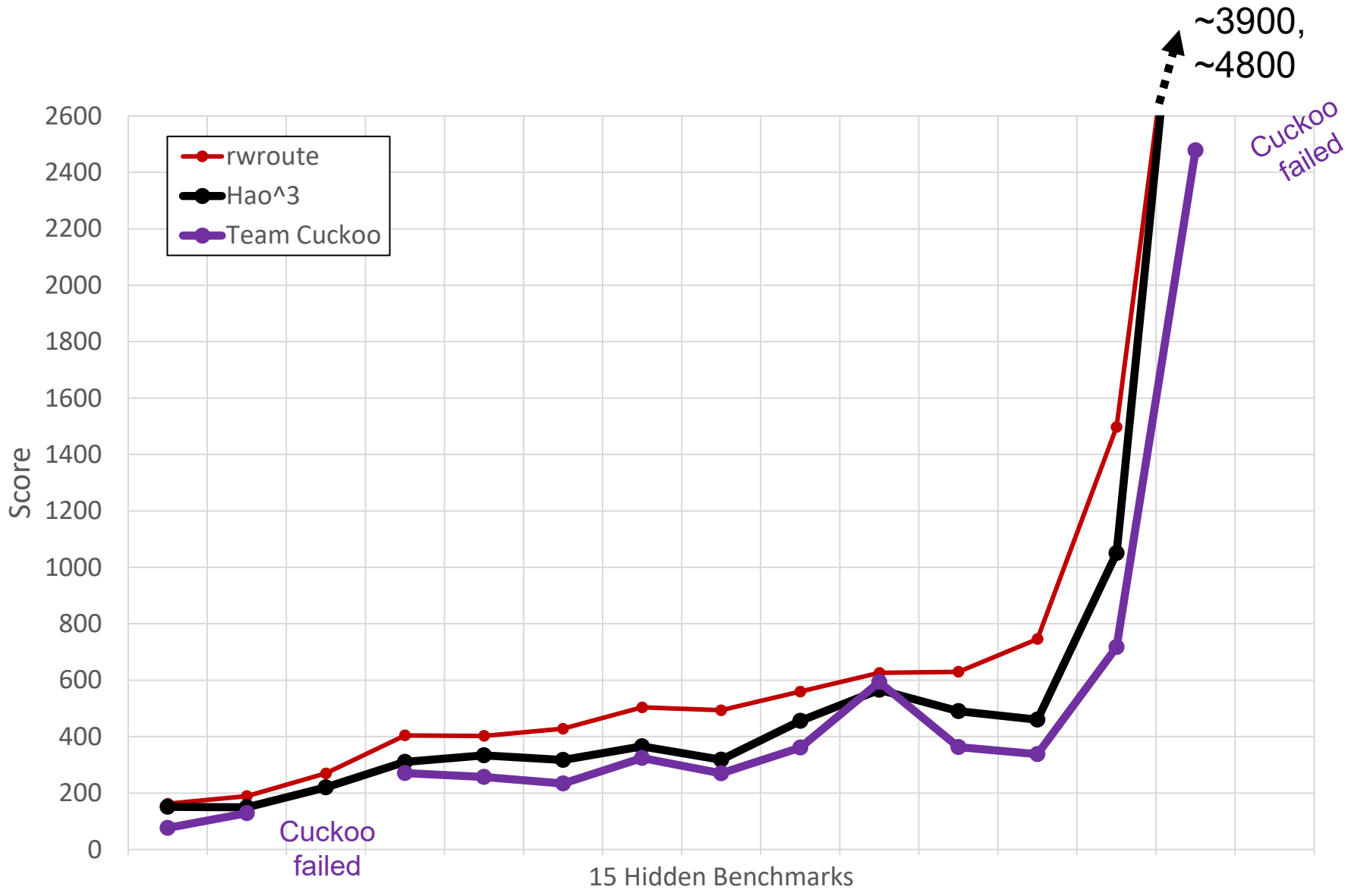
Contest Results



Contest Results

5th Place: **Hao^3**
(USTC)
Avg. Rank: 5.00

4th Place: **Team Cuckoo**
(PKU)
Avg. Rank: 4.27



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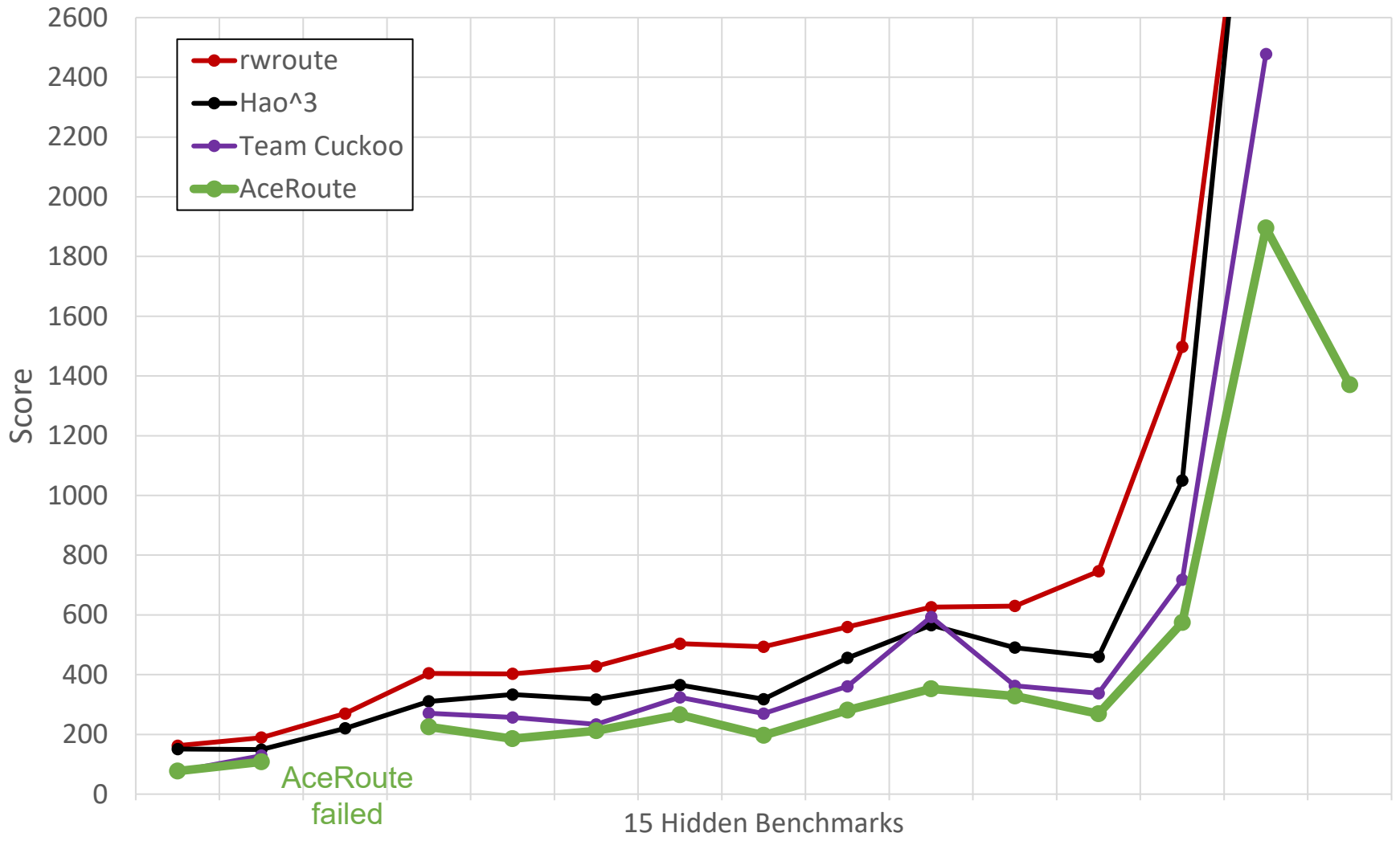

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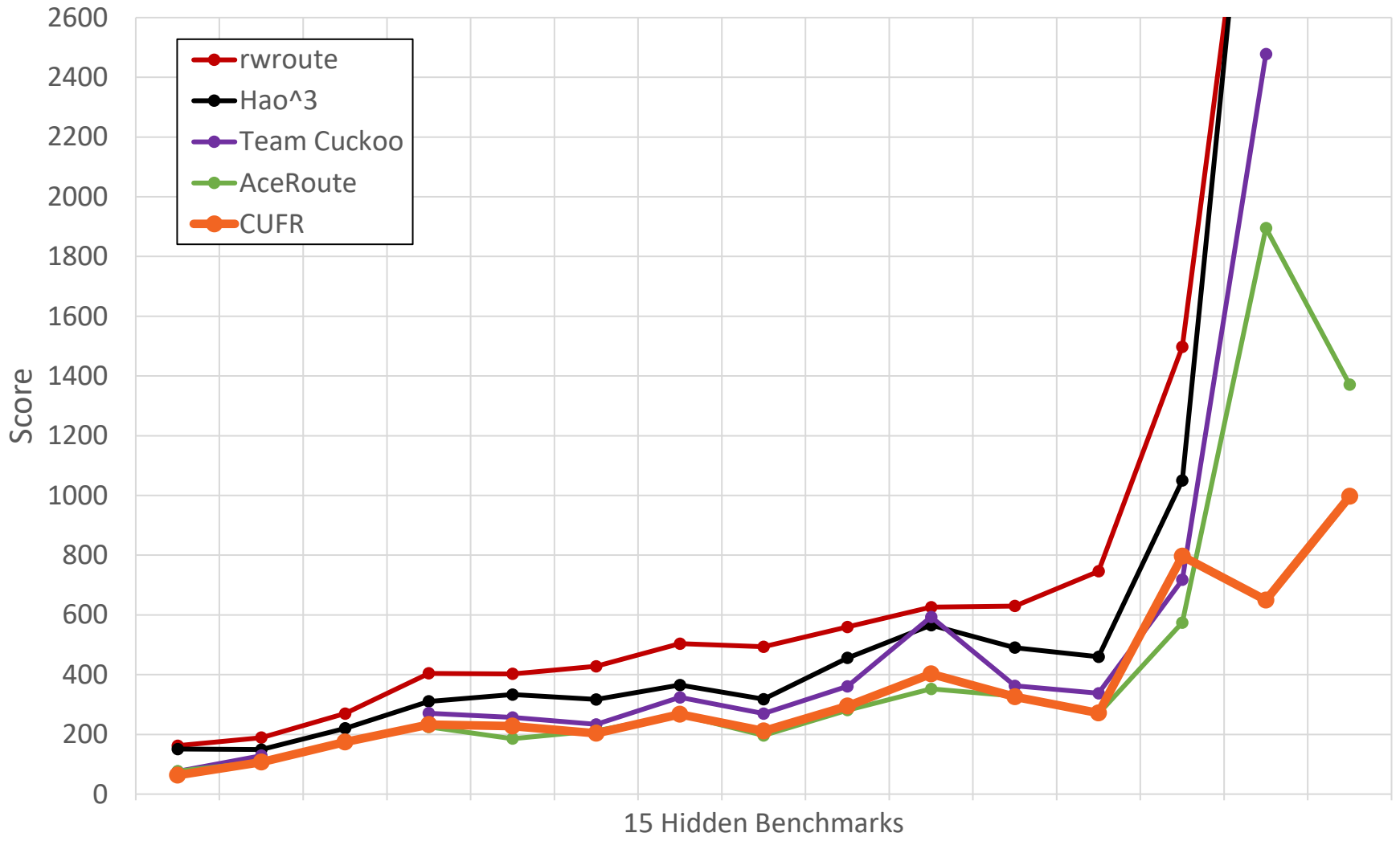

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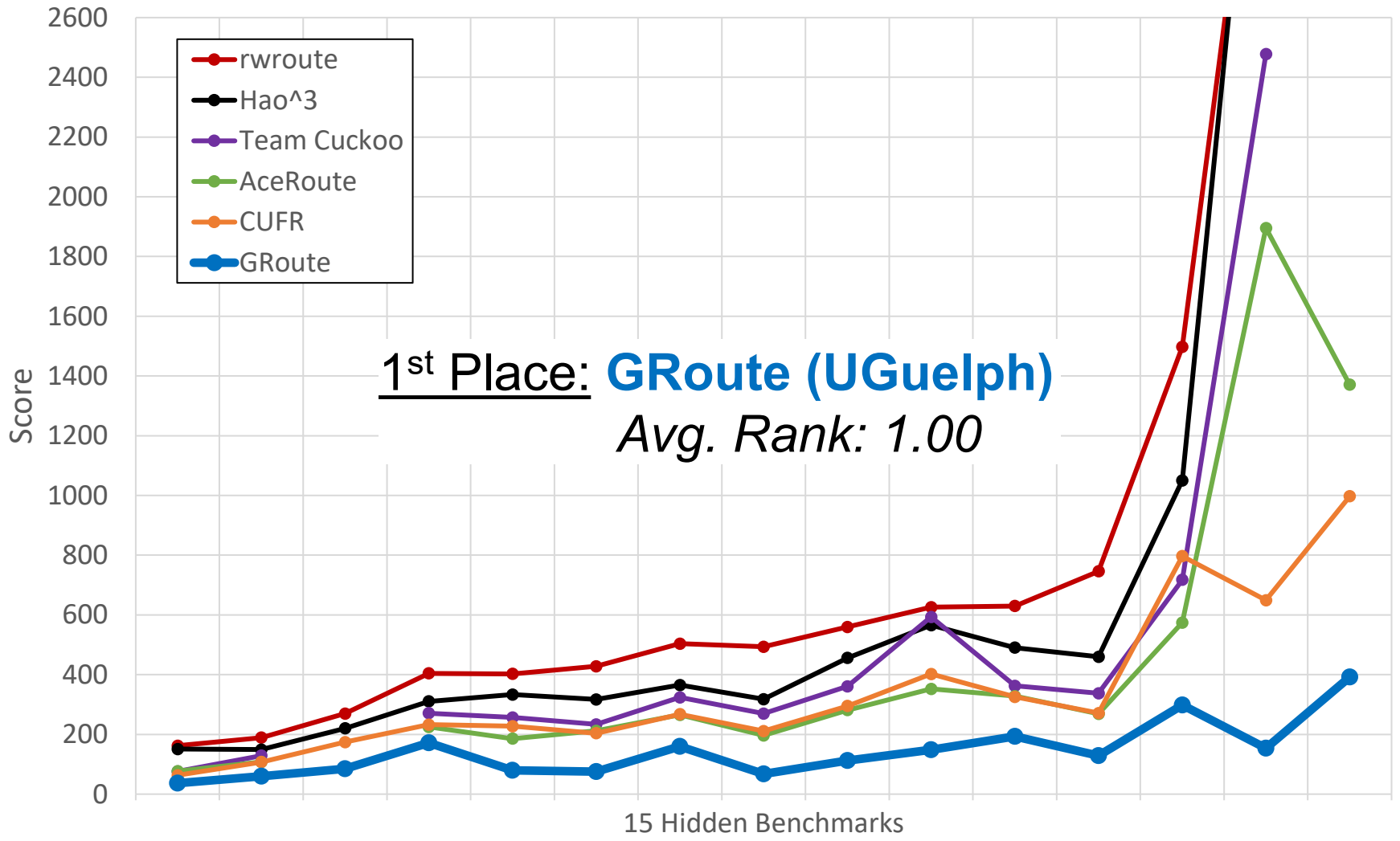
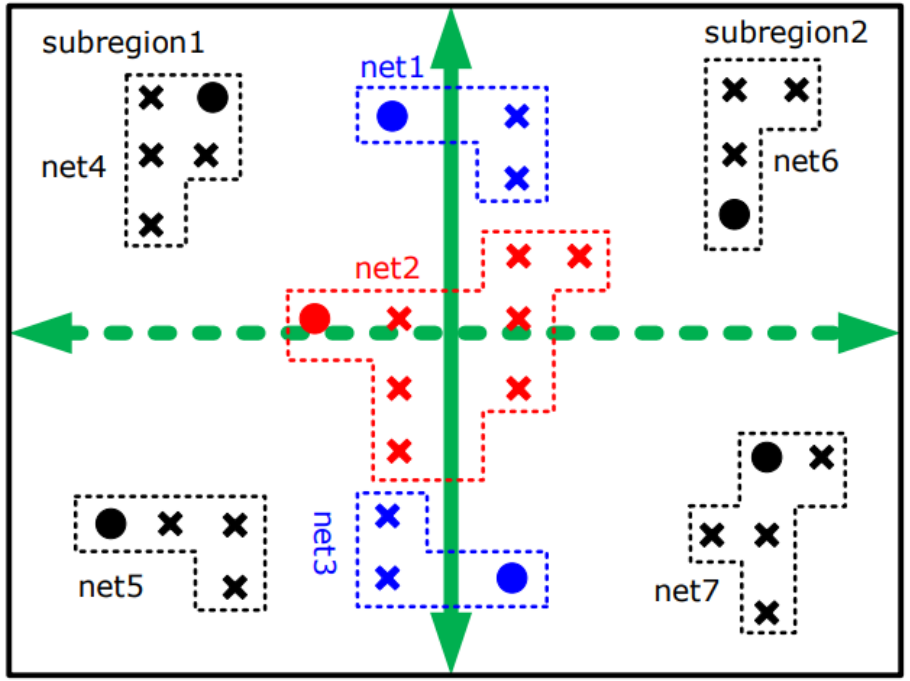


Behind The Scenes

- All PathFinder (1995) based!
  - 2 teams improve on RWRoute
  - 3 teams built a custom router
- Parallelism through:
  - Recursive bi-partitioning of device
  - Bounding box aware parallel scheduling
- More:
  - Tolerate overlaps initially (GRoute)
  - Hybrid update of congestion coefficients (CUFR)
  - Bidirectional A* search (AceRoute)
  - Details on contest website



(figure from AceRoute slide)

Final Thoughts

- More room for improvement: leverage GPU acceleration!
  - Honorable mention: Daniel Kluss (Archeo Futurus) -- used all four GPUs; didn't finish by deadline

- Hidden benchmark suite will be released
- 1 slide summary and short videos with more details from top 5 teams:

https://xilinx.github.io/fpga24_routing_contest

Thank you to all contest participants!!

Acknowledgements

- ISFPGA Organizers (in particular Zhiru Zhang, Aman Arora)

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- AMD RAD (Nicholas Fraser, Jakoba Petri-Koenig, Thomas Preusser)
- AMD AECG (Ismail Bustany)

- Shashwat Shrivastava (EPFL)

- HACC administrators at ETH Zurich, Paderborn University, National University of Singapore

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